

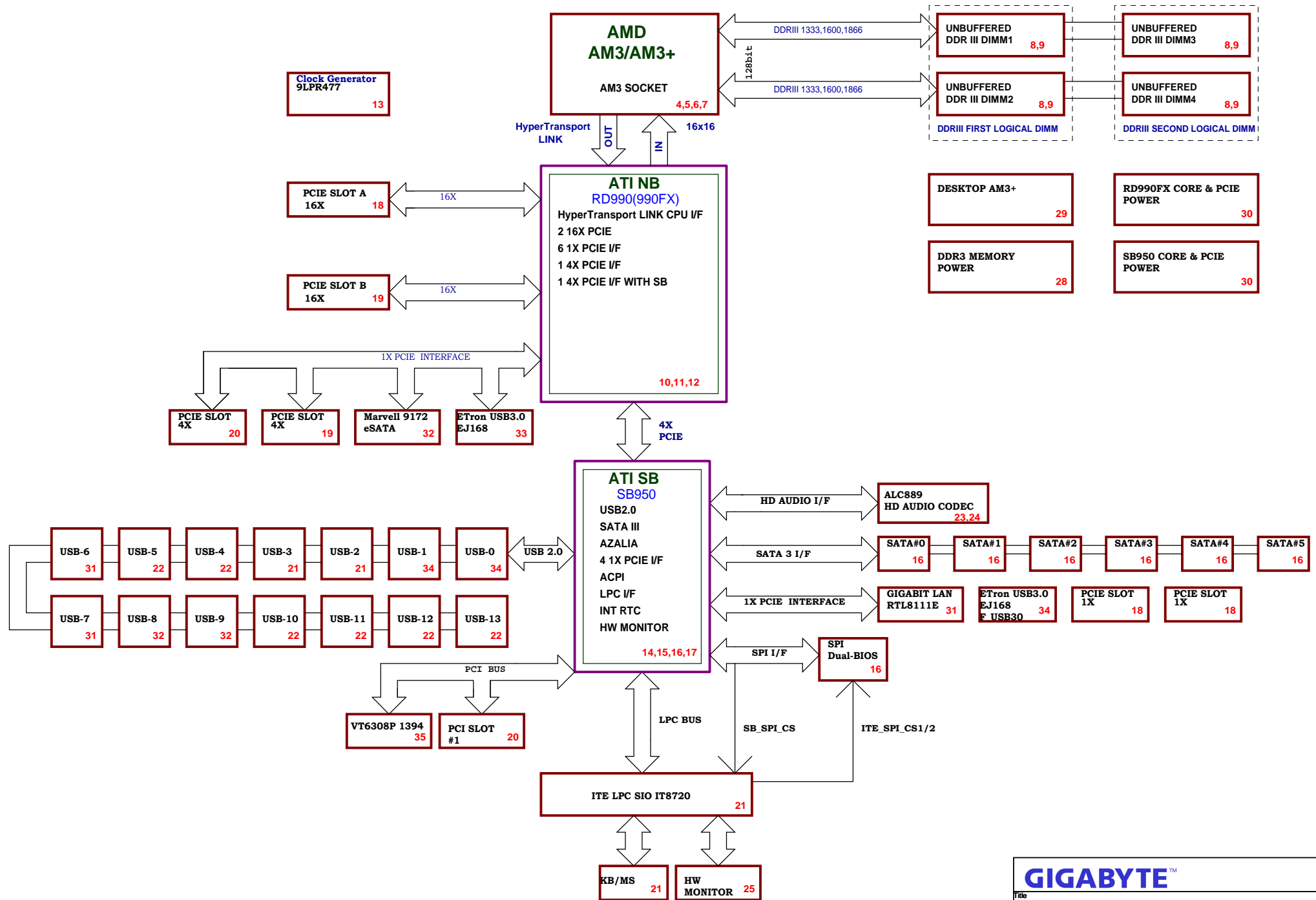
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21	IT8720 LPC, KB/MS, TPM
22	F_USB, IPWR
23	ALC889
24	AUDIO JACK
25	FAN/HWMO/COM

[illegible]

[illegible][illegible][illegible][illegible][illegible]

5					4					3					2					1																								
www.xinxunwei.com 400-800-9990															AM2-->AM3 Different: AE9-->AE7, H22-->H20. Extra pin:B2 AM3 socket is 938 pins. Only shift 2 pins.																													
Model Name:GA-990FXA-UD3										Circuit or PCB layout change for next version																																		
Component value change history										Version: 1.0 P-Code: U98145-0																																		
4 Layer, 4mil 50ohm +/- 15% X																																												
Date					Version					Change Items																																		
2011.03.17					0.1 New BOM Release.					PCB:0.1					Modify from 9M990FXA5-00-01																													
2011.04.13					1.0A BOM Release.					PCB:1.0					Add AMD Validation parts ,Add Thermal-Die schematic Delete AZ2025 for AUDIO																													
2011.04.27					1.0B BOM Release.					PCB:1.01					Remove PCB silkscreen SLI logo																													
2011.05.05					1.0C BOM Release.					PCB:1.01					更改 CPU RM 為分離式																													
2011.05.05					1.0D BOM Release.					PCB:1.0					PCB Change to 1.0 (Silk W/SLI Logo)																													

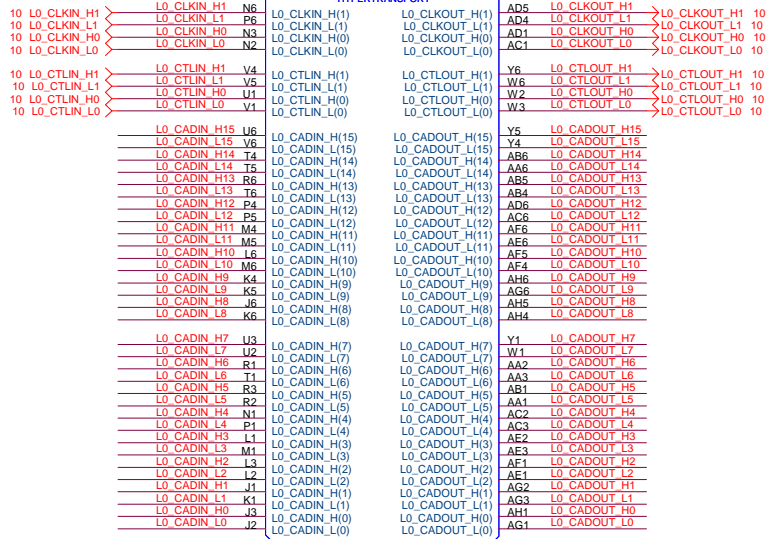
**GIGABYTE™**

Title			BLOCK DIAGRAM	
Size	Document Number	Rev		
Custom	GA-990FXA-UD3	1.0		
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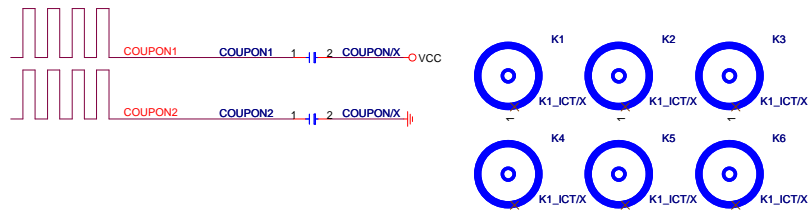
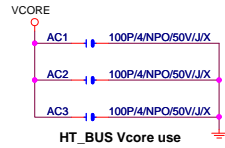
L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

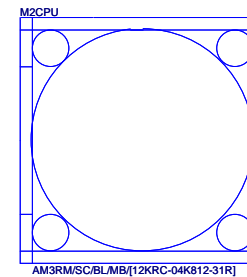
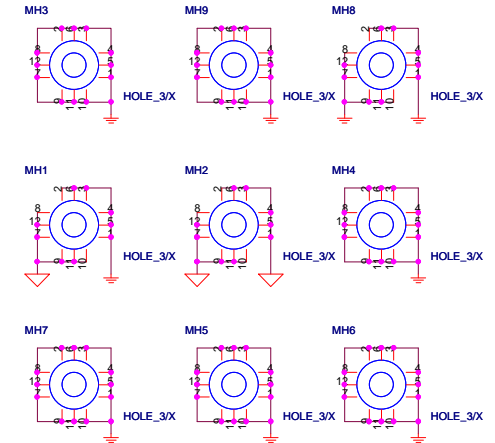


CPU-SK941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

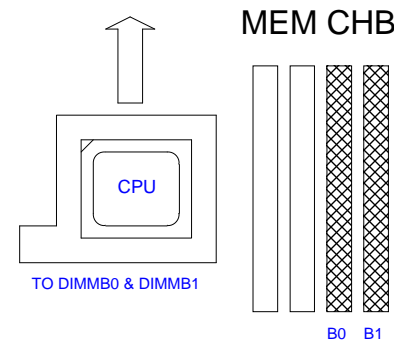
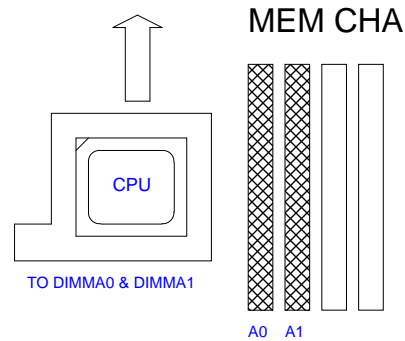
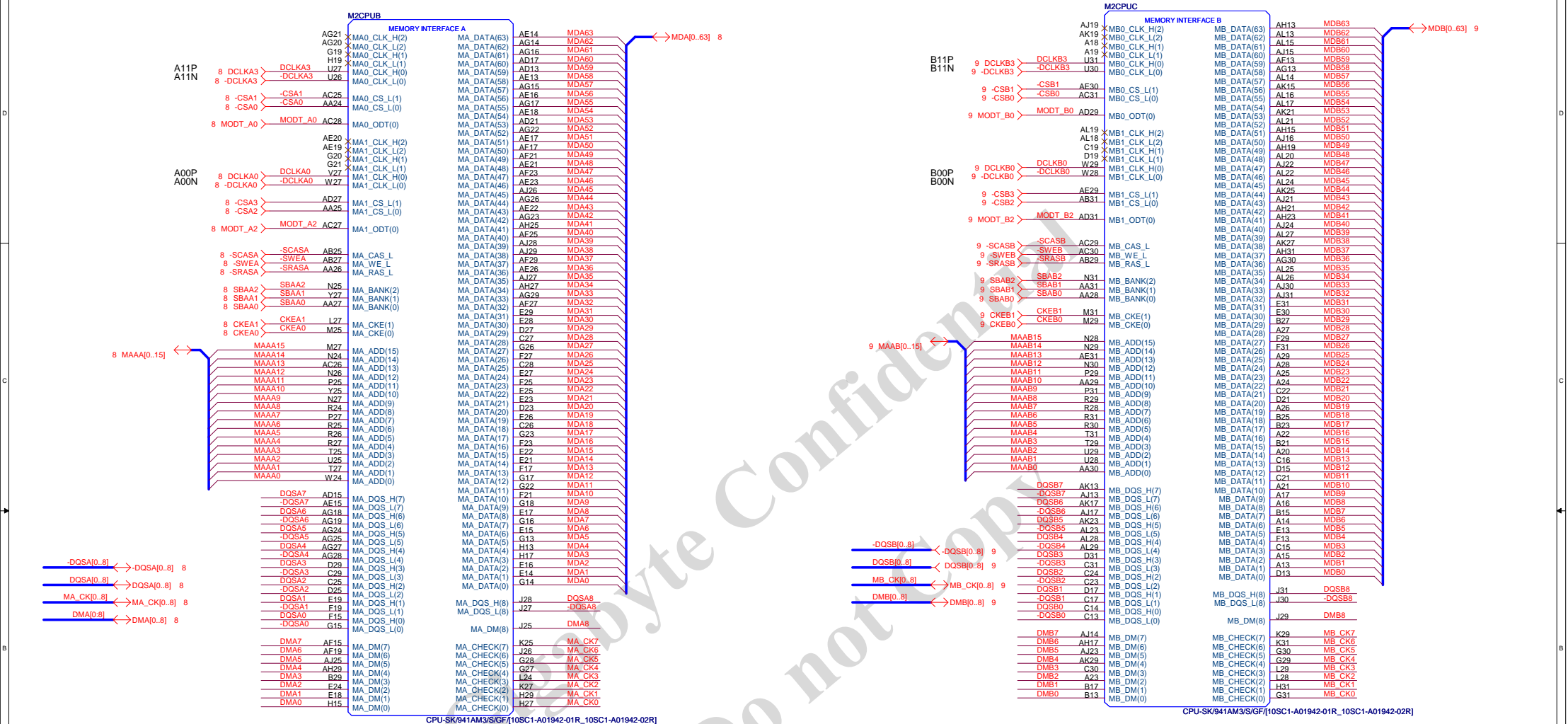


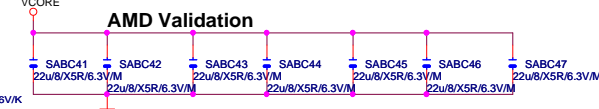
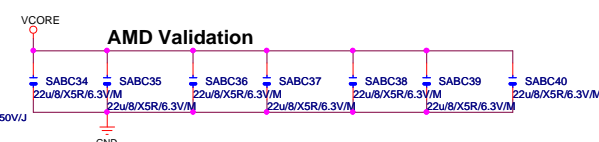
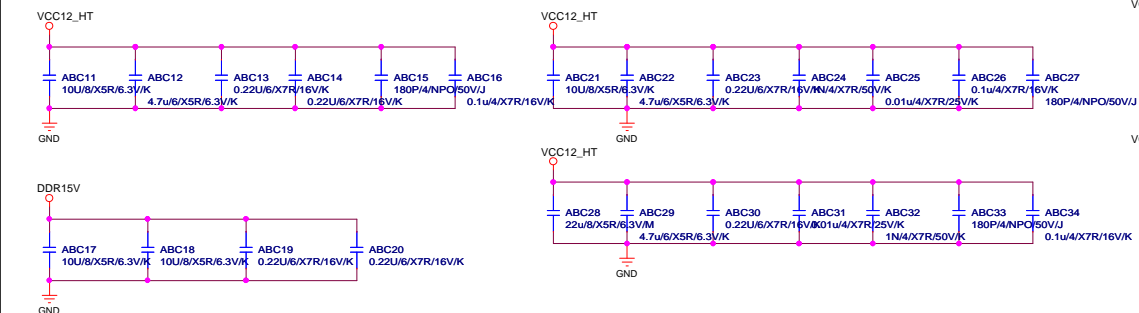
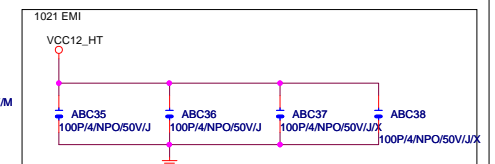
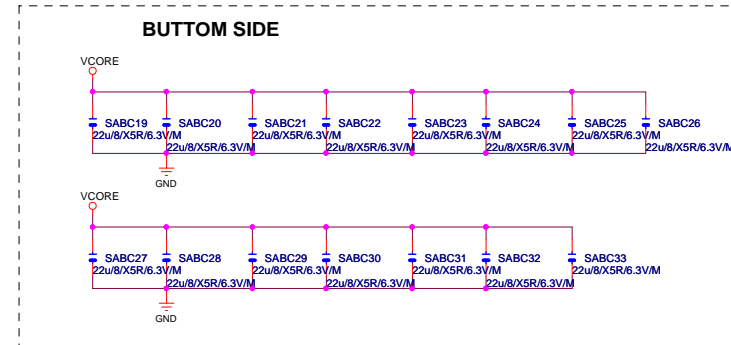
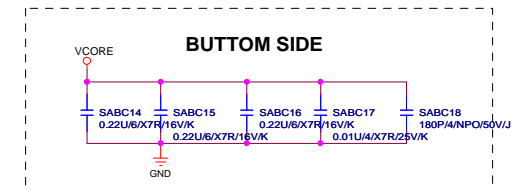
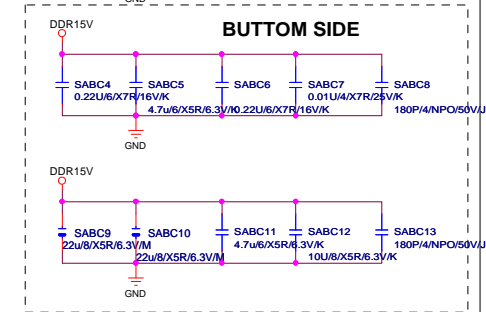
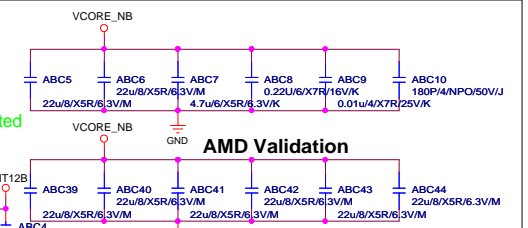
CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

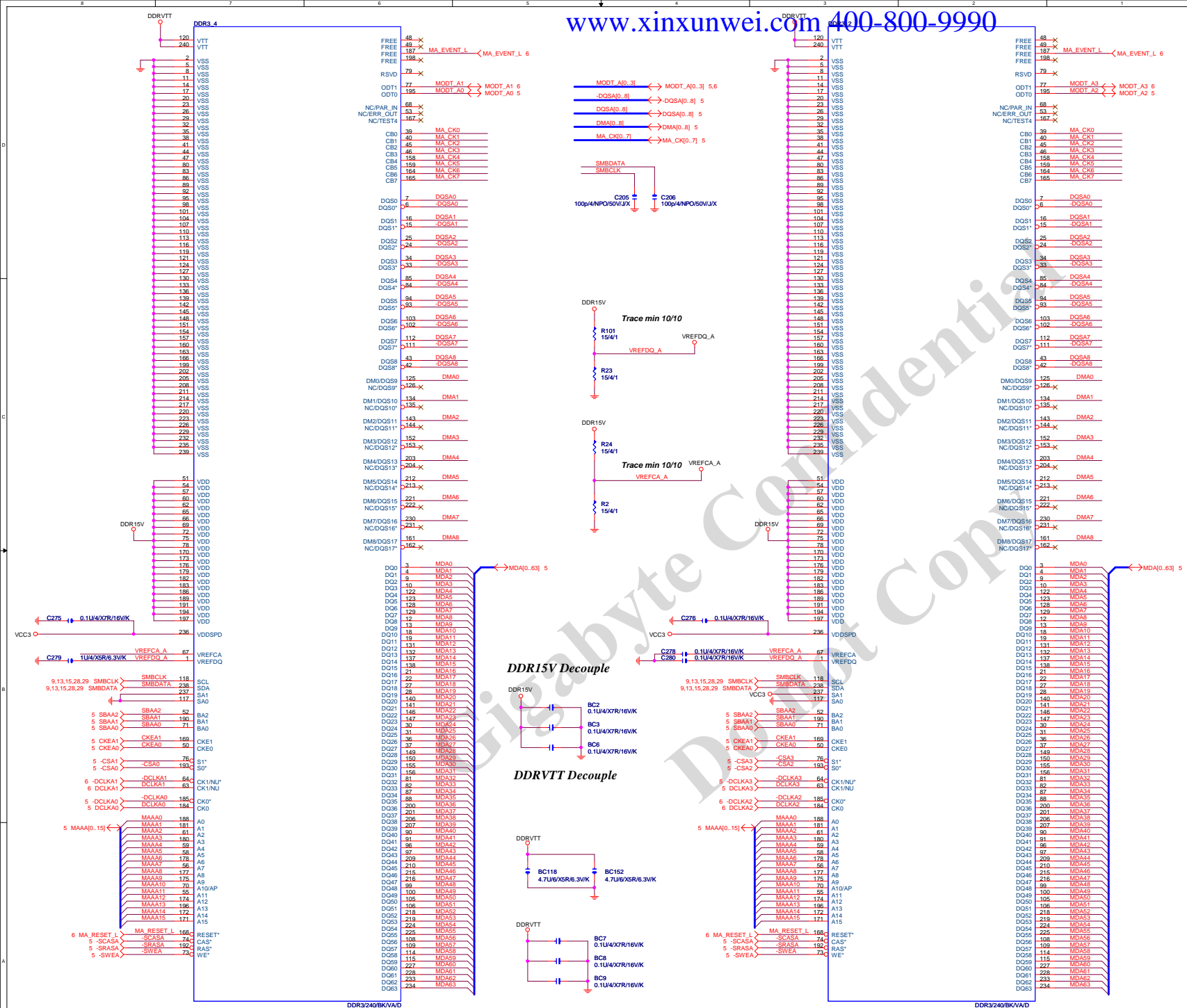
VLDT_A = VCC12_HT
 VLDT_B = HT12B

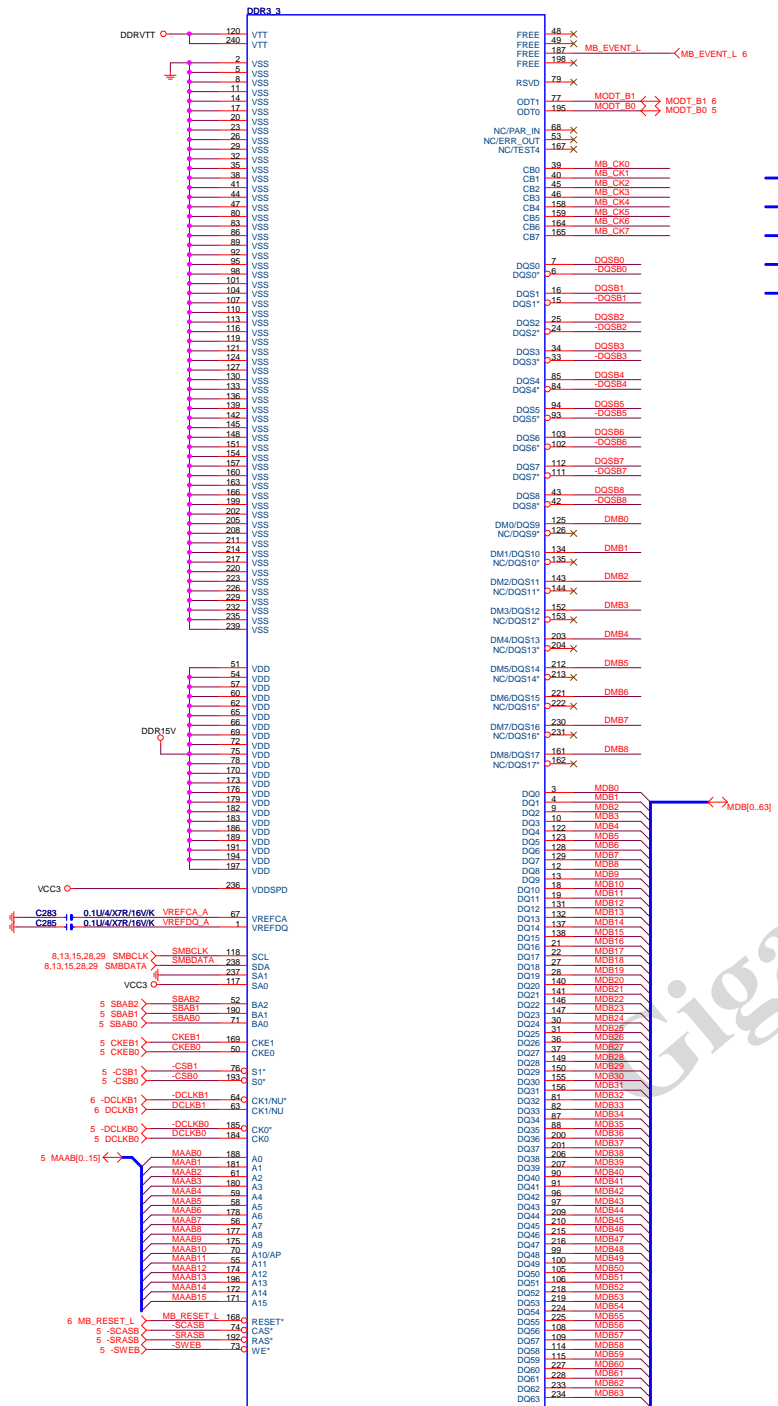


GIGABYTE		
Title COVER SHEET		
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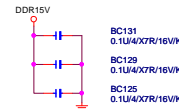




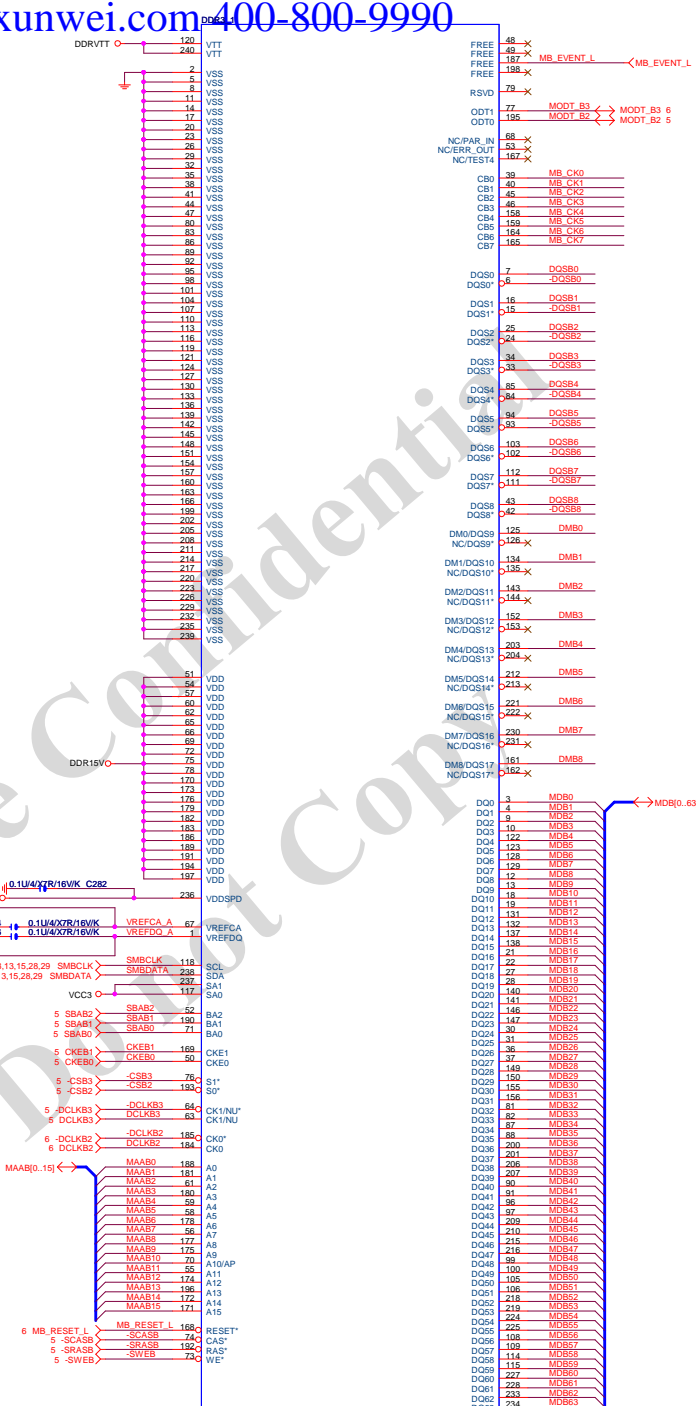
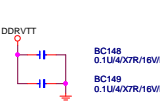




DDR15V Decouple



DDRVTT Decouple

**GIGABYTE**

PART 1/5

PART 2/5

HYPERTRANSPORT IF

PCIE GPP1

PCIE GPP2

PCIE ALINK



PLACE THESE CAP CLOSE TO CONNECTOR

PCI E slot TX need CAP close to slot side

PLACE THESE CAP CLOSE TO CONNECTOR

PLACE THESE CAP CLOSE TO NB.

GIGABYTE™

RD990 HT & GFX I/F

Size	Document Number	Rev
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L0_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	L0_CADIN_H15
L0_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	L0_CADIN_L15
L0_CADOUT_H14	U24	HT_RXCAD14P	HT_TXCAD14P	M25	L0_CADIN_H14
L0_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M24	L0_CADIN_L14
L0_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	L0_CADIN_H13
L0_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	L0_CADIN_L13
L0_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	L0_CADIN_H12
L0_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	L0_CADIN_L12
L0_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	L0_CADIN_H11
L0_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	L0_CADIN_L11
L0_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	L0_CADIN_H10
L0_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	L0_CADIN_L10
L0_CADOUT_H9	AC24	HT_RXCAD9P	HT_TXCAD9P	F24	L0_CADIN_H9
L0_CADOUT_L9	AC23	HT_RXCAD9N	HT_TXCAD9N	F25	L0_CADIN_L9
L0_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	L0_CADIN_H8
L0_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	L0_CADIN_L8
L0_CADOUT_H7	T28	HT_RXCAD7P	HT_TXCAD7P	N26	L0_CADIN_H7
L0_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	N27	L0_CADIN_L7
L0_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M27	L0_CADIN_H6
L0_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	M28	L0_CADIN_L6
L0_CADOUT_H5	V28	HT_RXCAD5P	HT_TXCAD5P	L26	L0_CADIN_H5
L0_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	L27	L0_CADIN_L5
L0_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K27	L0_CADIN_H4
L0_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	K28	L0_CADIN_L4
L0_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	H27	L0_CADIN_H3
L0_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	H28	L0_CADIN_L3
L0_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	G26	L0_CADIN_H2
L0_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	G27	L0_CADIN_L2
L0_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	F27	L0_CADIN_H1
L0_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	F28	L0_CADIN_L1
L0_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P	E26	L0_CADIN_H0
L0_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N	E27	L0_CADIN_L0

4 L0_CLKOUT_H1	L0_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4 L0_CLKOUT_L1	L0_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4 L0_CLKOUT_H0	L0_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
4 L0_CLKOUT_L0	L0_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4

4 L0_CTLOUT_H1	L0_CTLOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	L0_CTLIN_H1	L0_CTLIN_H1	4
4 L0_CTLOUT_L1	L0_CTLOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	L0_CTLIN_L1	L0_CTLIN_L1	4
4 L0_CTLOUT_H0	L0_CTLOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P27	L0_CTLIN_H0	L0_CTLIN_H0	4
4 L0_CTLOUT_L0	L0_CTLOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P28	L0_CTLIN_L0	L0_CTLIN_L0	4

SNR0	1.21K/4/1	HT_RXCALP	D25	HT_RXCALP	D24	HT_RXCALN	HT_TXCALN	NR1	1.21K/4/1
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L0_CADIN_H0[15]	L0_CADIN_H0[15]	4
L0_CADIN_L0[15]	L0_CADIN_L0[15]	4
4 L0_CADOUT_H0[15]	L0_CADOUT_H0[15]	
4 L0_CADOUT_L0[15]	L0_CADOUT_L0[15]	

EXP_A_RXP0[15]	EXP_A_RXP0[15]	18
EXP_A_RXN0[15]	EXP_A_RXN0[15]	18
EXP_A_TXP0[15]	EXP_A_TXP0[15]	18
EXP_A_TXN0[15]	EXP_A_TXN0[15]	18

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

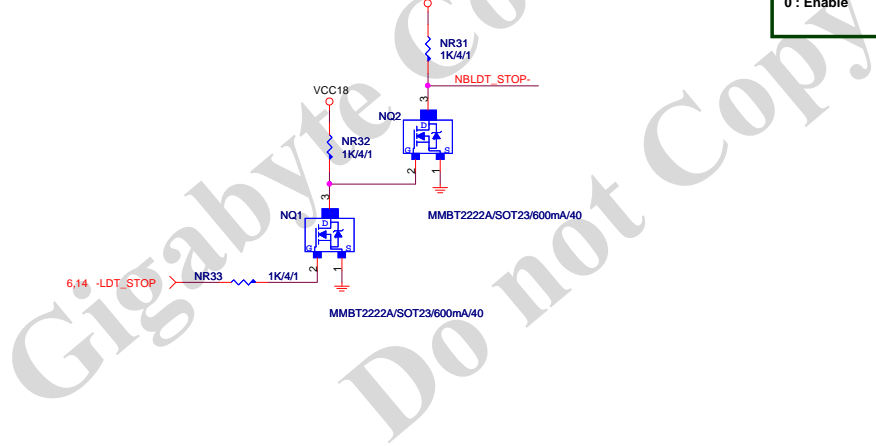
EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19

EXP_B_RXP0[15]	EXP_B_RXP0[15]	19
EXP_B_RXN0[15]	EXP_B_RXN0[15]	19

EXP_B_TXP0[15]	EXP_B_TXP0[15]	19
EXP_B_TXN0[15]	EXP_B_TXN0[15]	19



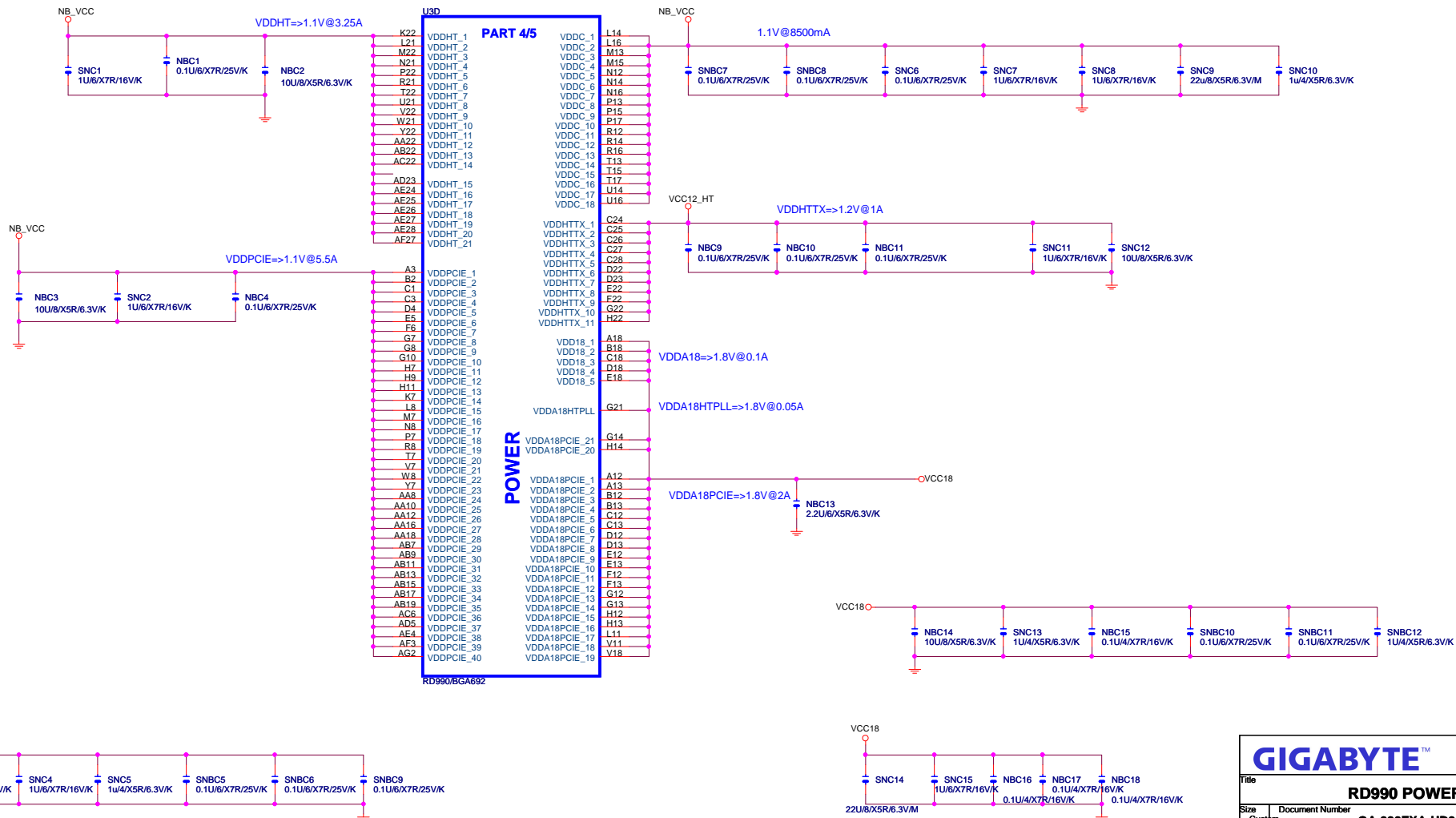
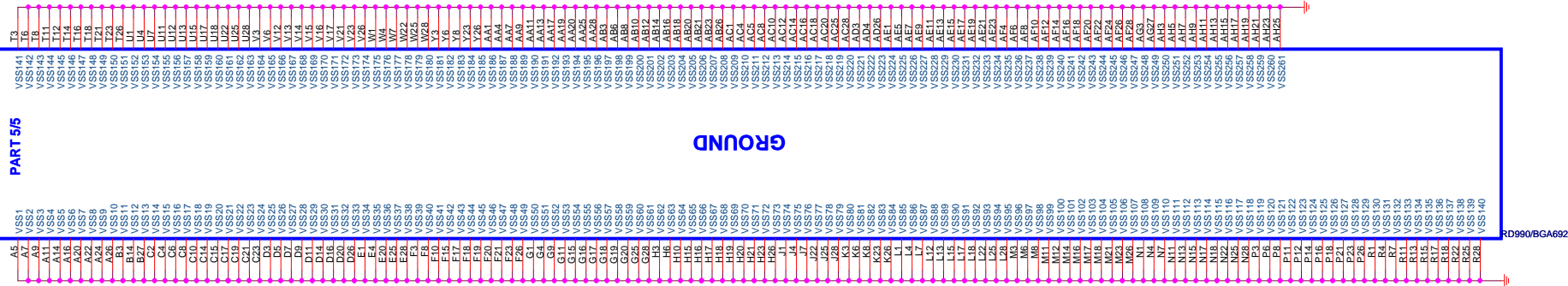
Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

These pin straps are used to configure PCI-E GPP mode.

DFT_GPIO1: LOAD_EEPROM_STRAPS

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

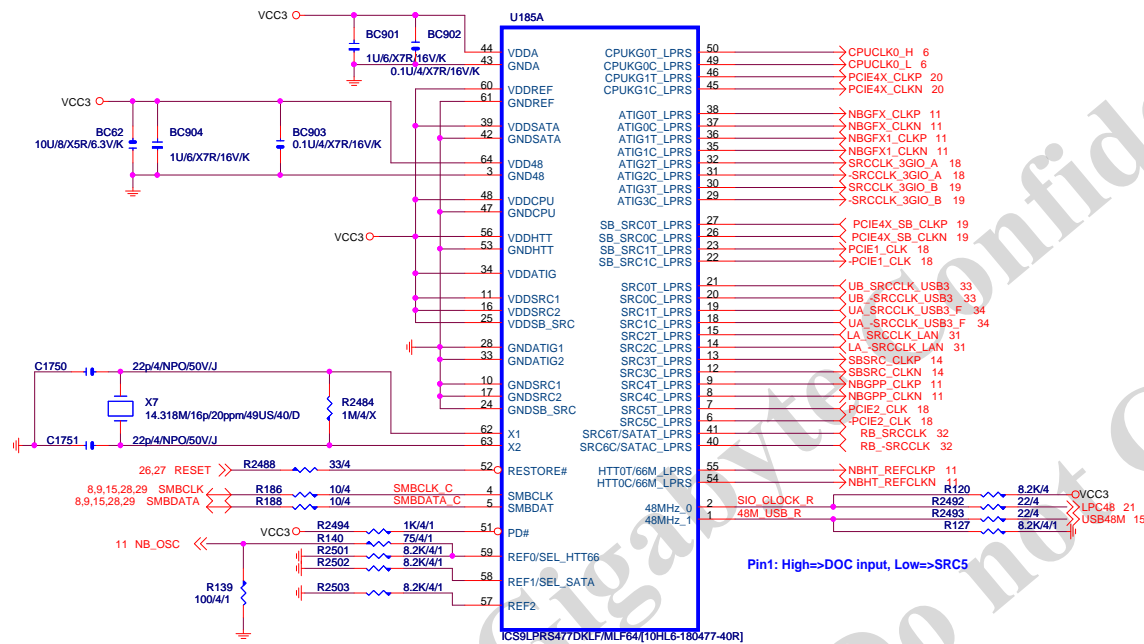
Enables the Test Debug Bus using PCIe bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable



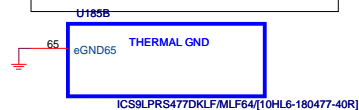
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

IMC_GPIO200 PR61 2.2K/4/1
IMC_GPIO199 PR62 2.2K/4/1

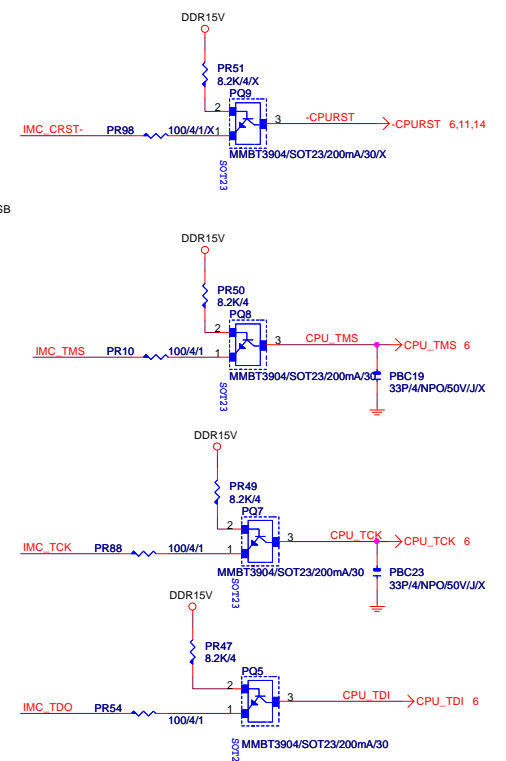
ROM TYPE:

H, H = Reserved

L, L = SPI ROM DEFAULT

L, H = LPC ROM

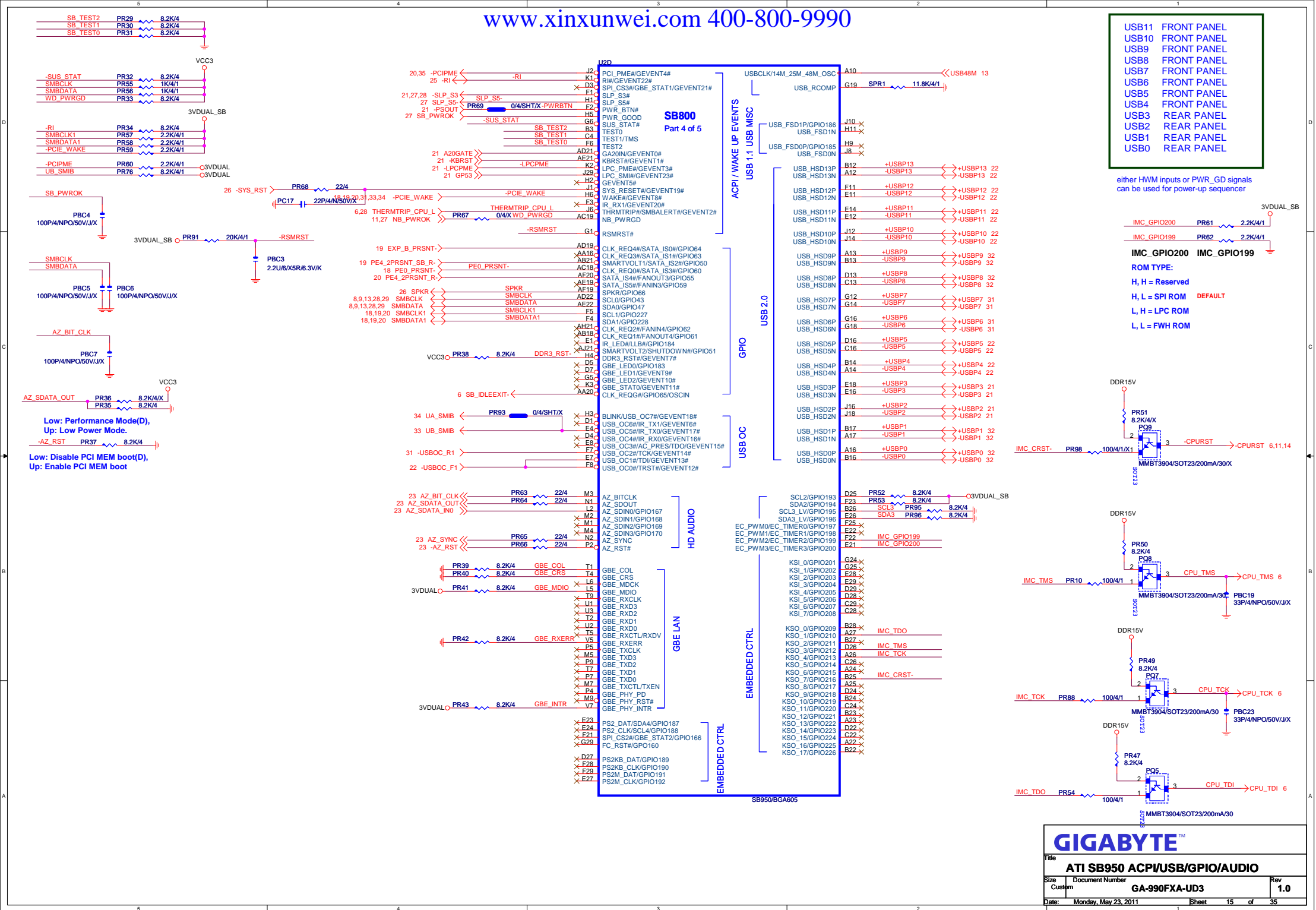
L, L = FWH ROM

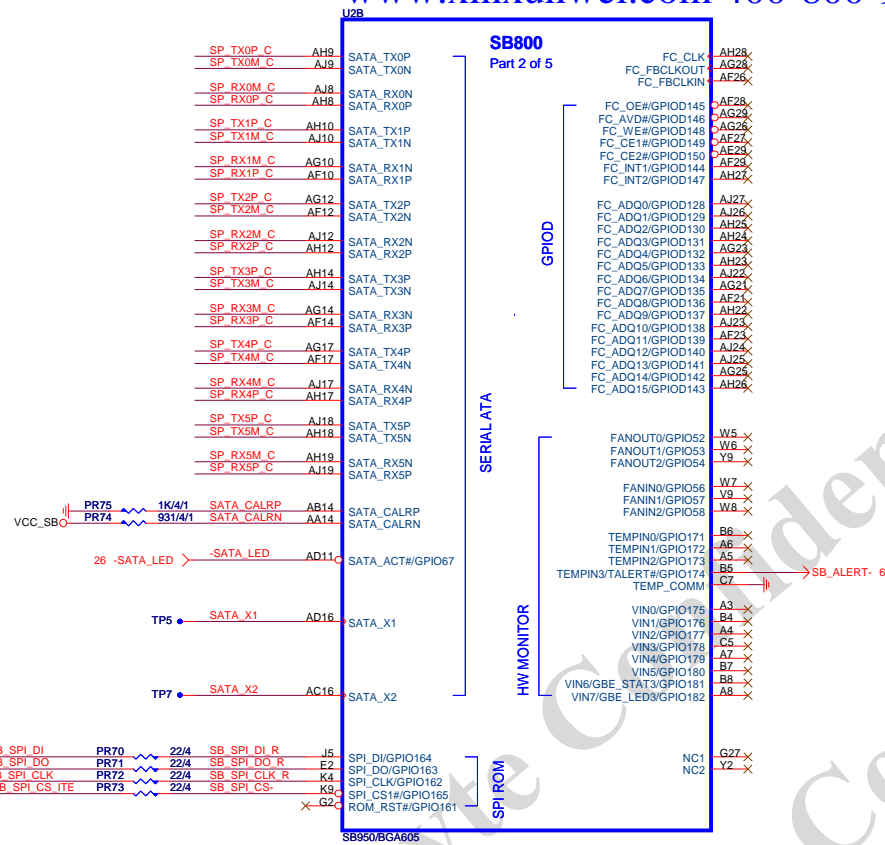


GIGABYTE™

ATI SB950 ACPI/USB/GPIO/AUDIO

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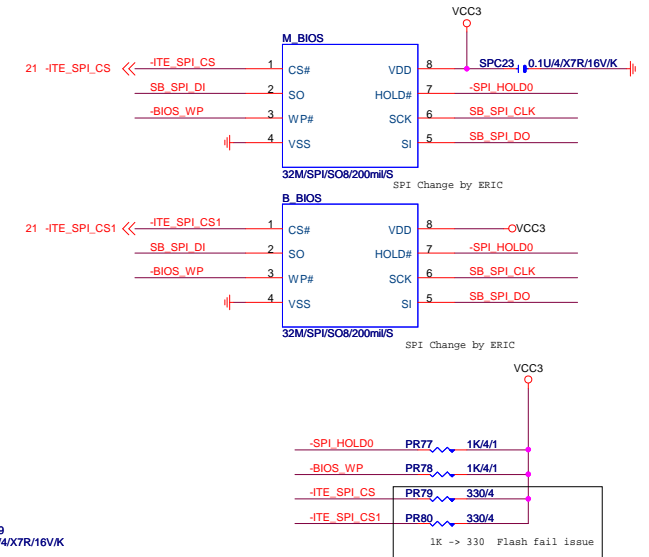
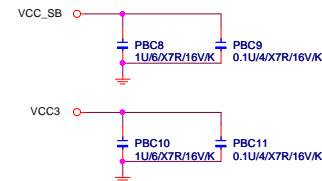
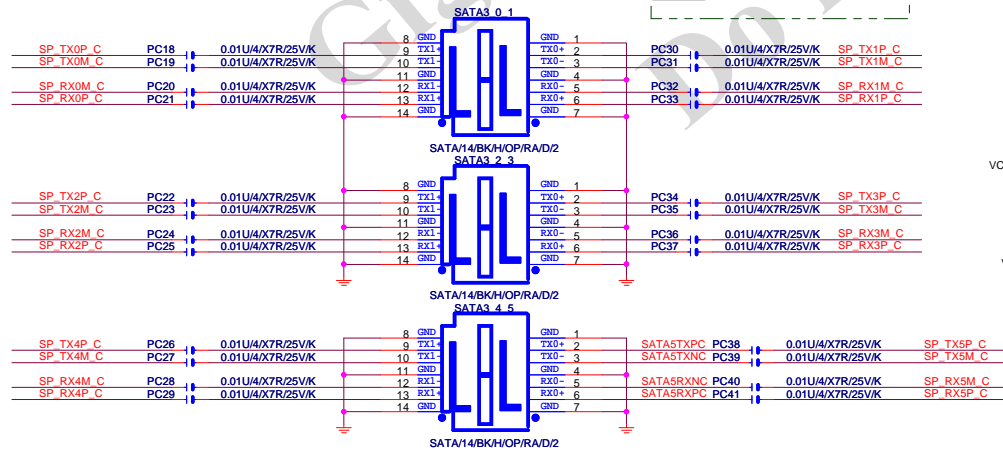
PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

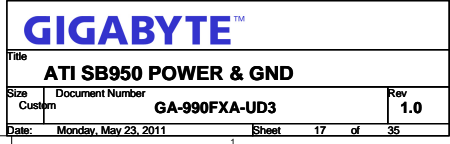


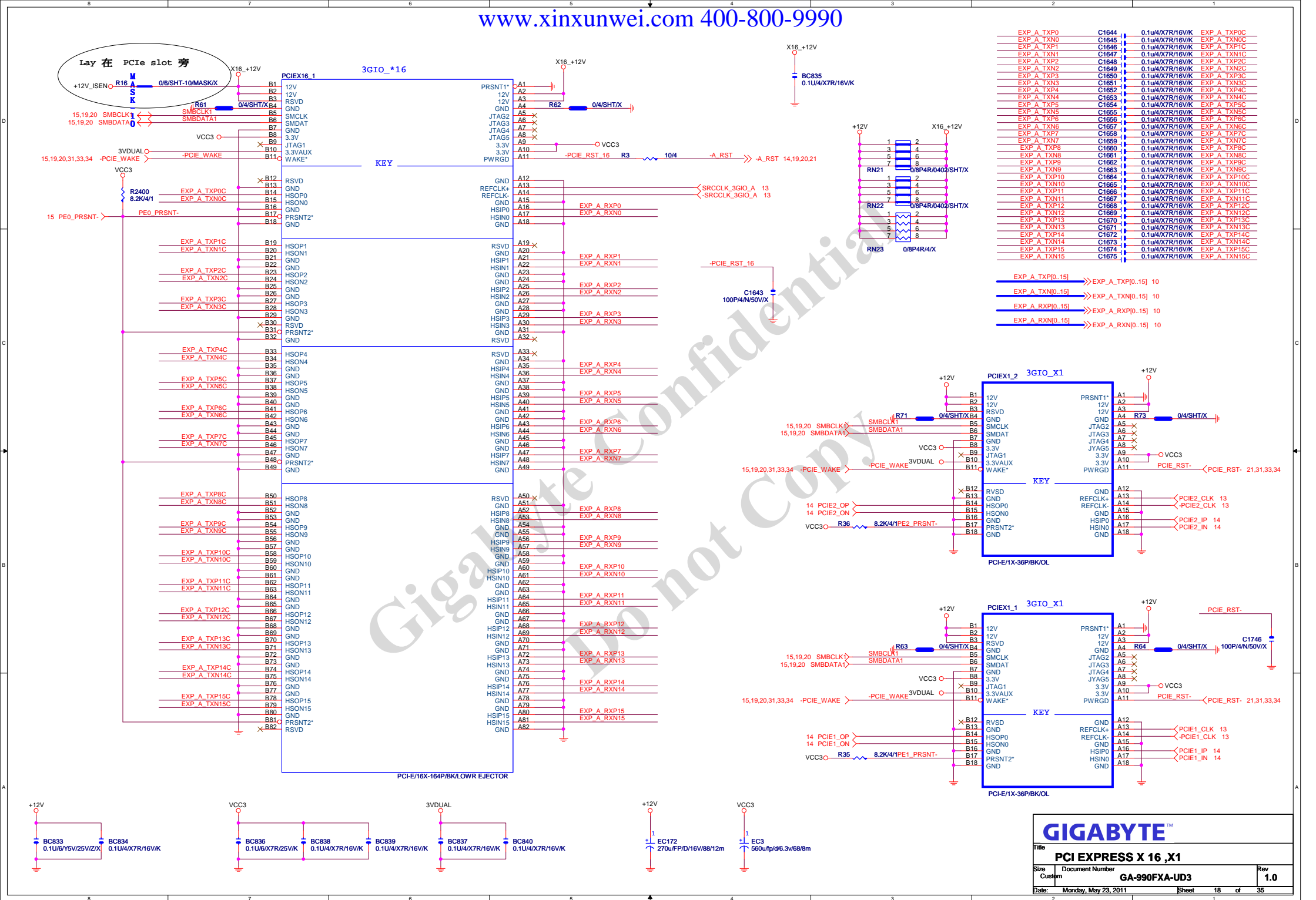
PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

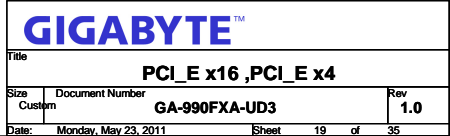


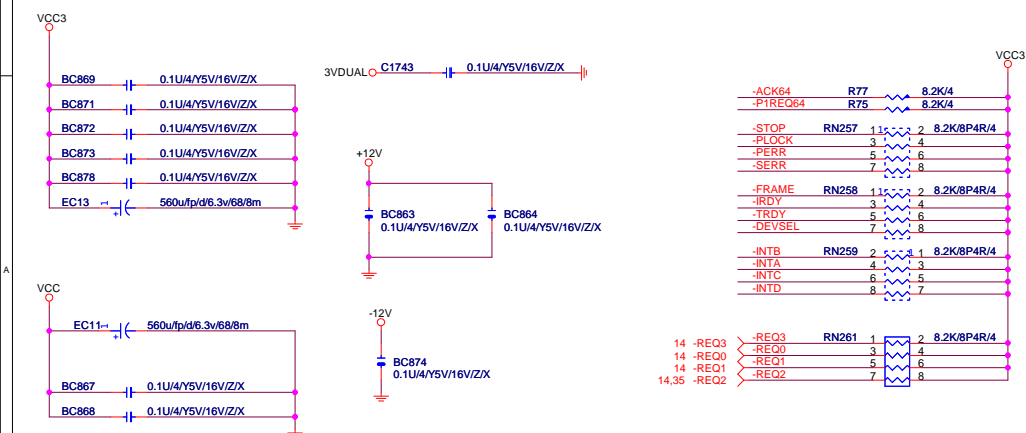
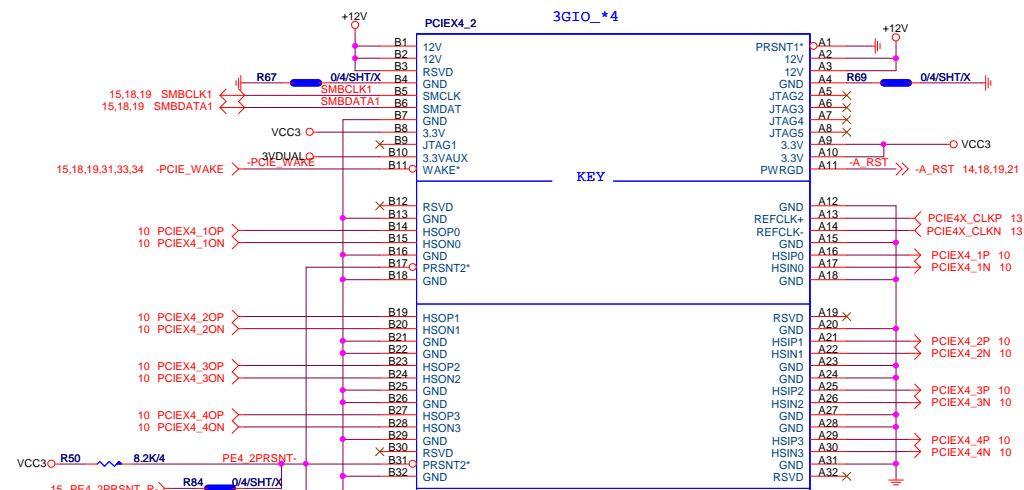
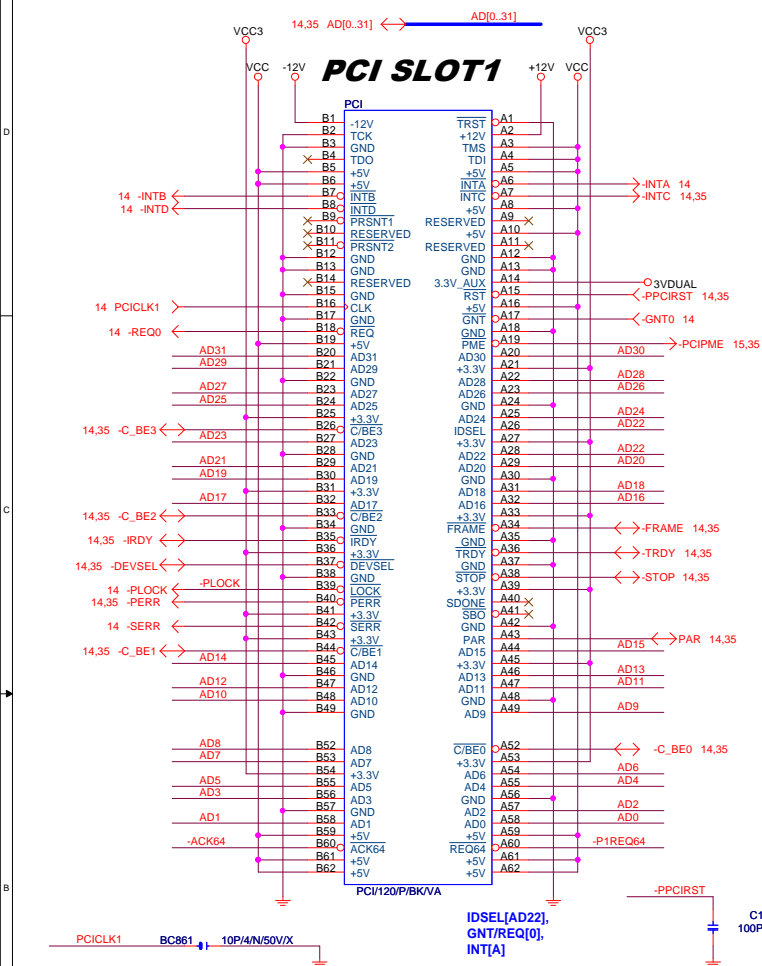
GIGABYTE

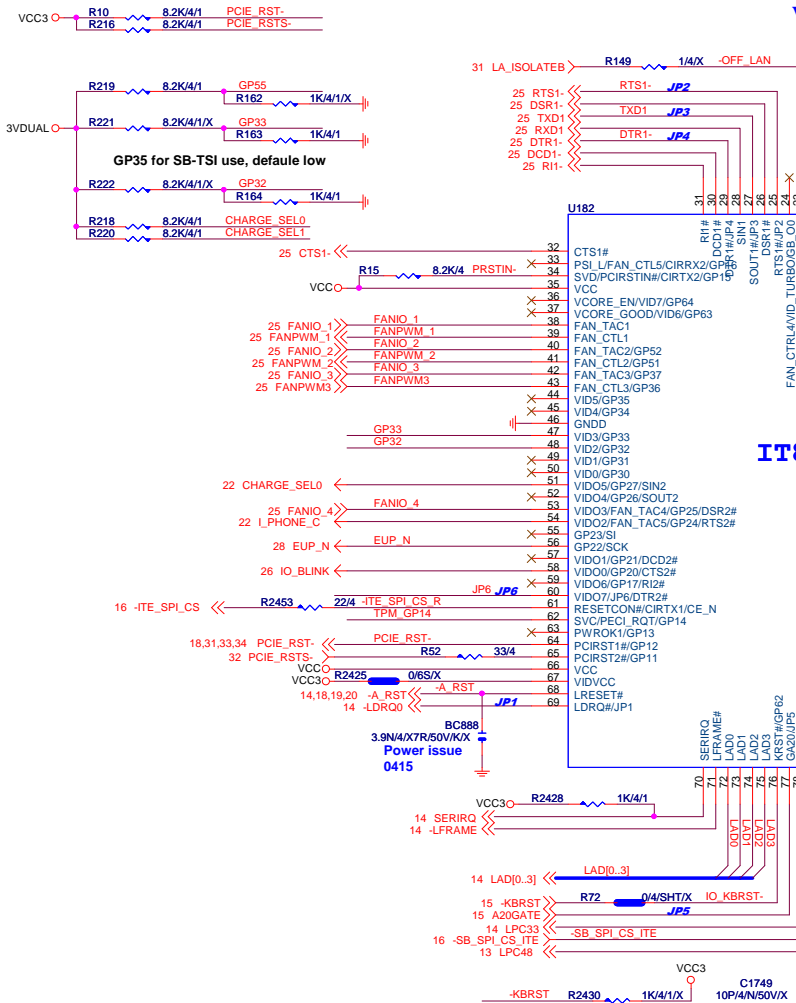
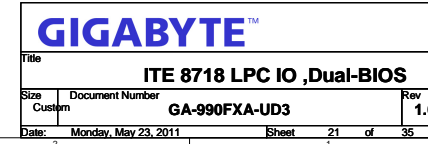
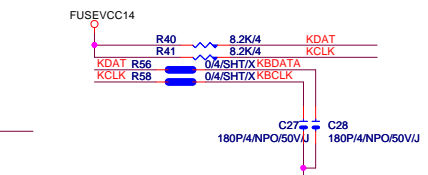
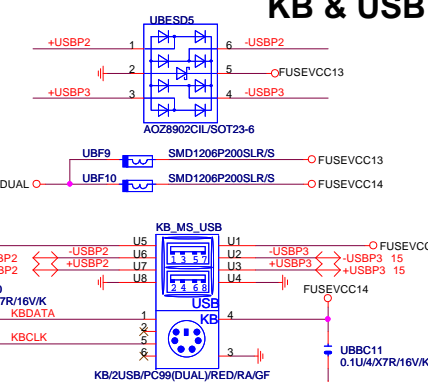
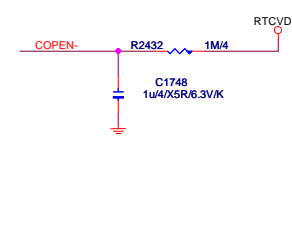
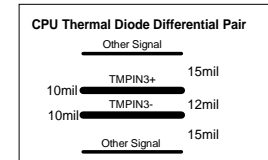
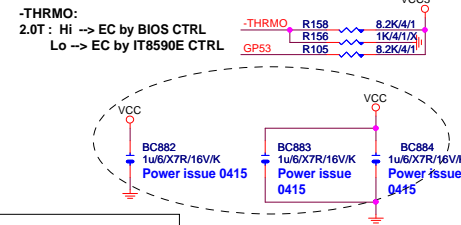
Title		
ATI SB950 SATA/IDE/HWM/SPI		
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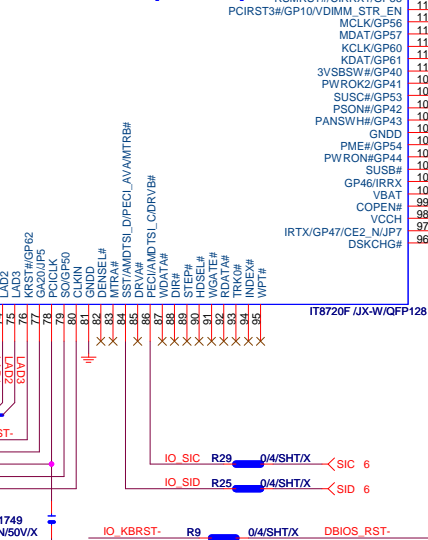






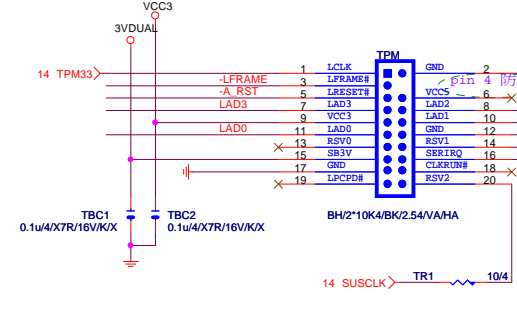
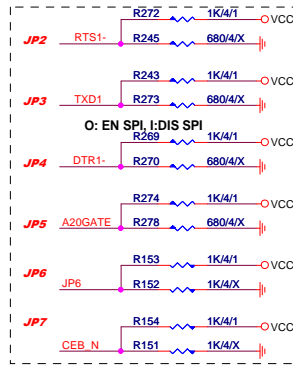


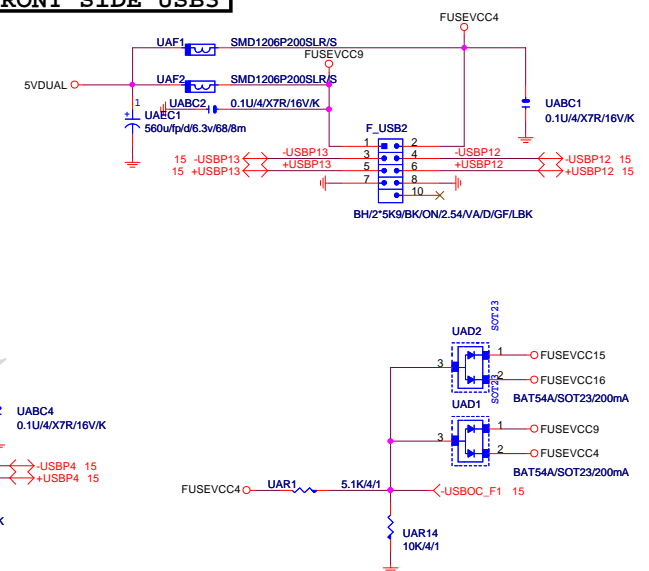
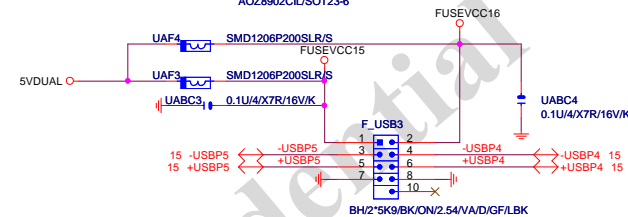
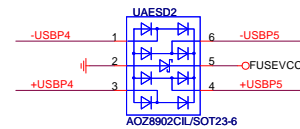
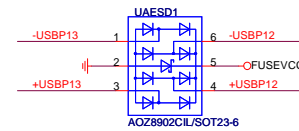
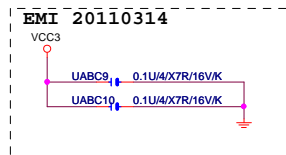
IT8720F (GB)



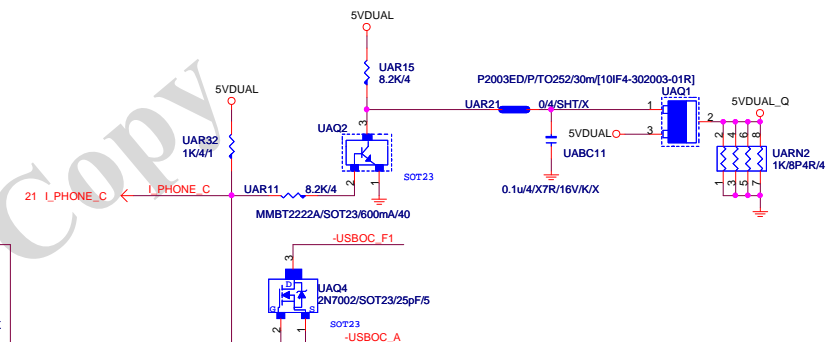
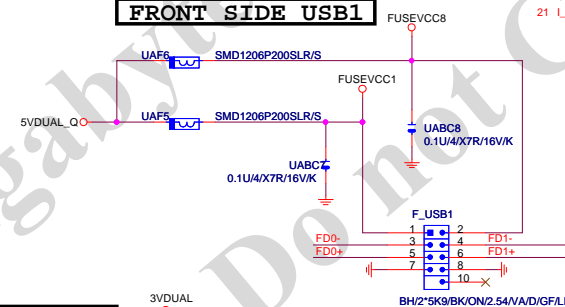
IT8720GB Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	1 Disabled.
Pin 69	Flash I/F Address Segment 1 is enabled	
JP2	VIDO_EN	1 Disable VID output pins
Pin 25	Enable VID output pins	
JP3	CHIP_SEL	Chip selection in Configuration
Pin 27		
JP4	K8PWR_EN	1 K8 power sequence disabled
Pin 29	0 K8 power sequence enabled	
JP3 & JP5	FAN_CTL_SEL	11 Half Run Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77	0 No Run Default value of EC Index 15h/16h/17h is 7Fh	
	01 Full Run Default value of EC Index 15h/16h/17h is 00h	
	00 75% Run Default value of EC Index 15h/16h/17h is 20h	
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin 77	0 Enable WDT to rest PWROK	
JP6	SVID_EN	1 Disable SVID Function
Pin 60	0 Enable SVID Function	
JP7	Dual_BIOS_EN	1 Enable Dual BIOS Function for GigaByte Only
Pin 97	0 Disable Dual BIOS Function for GigaByte Only	



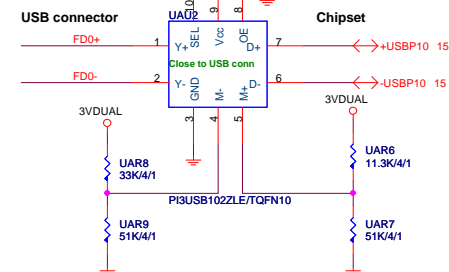


FRONT SIDE USB1

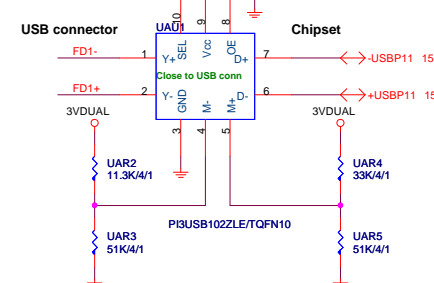


i_Phone charger circuit

21 CHARGE_SEL0
DEFAULT H, STABBY POWER



21 CHARGE_SEL1
DEFAULT H, STABBY POWER

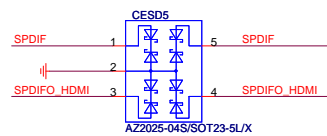
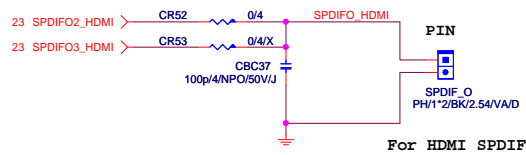
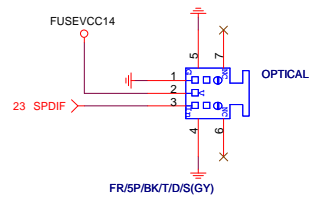
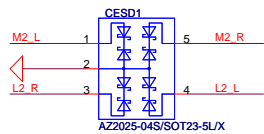
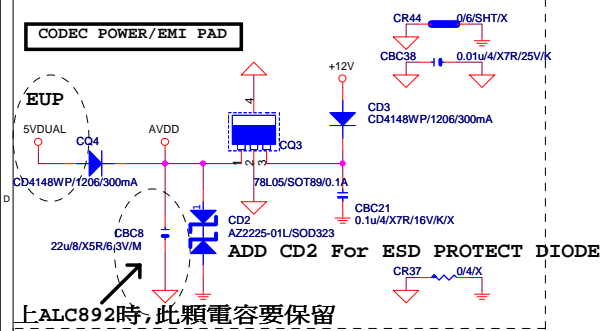


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Title			COM/LPT/F_USB
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	1.0	
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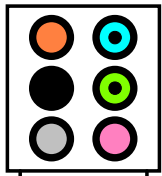
Gigabyte Technology			
Title		HD AUDIO ALC889A	
Size	Document Number	GA-990FXA-UD3	
Custom			Rev 1.0
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CODEC POWER/EMI PAD

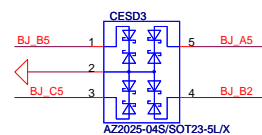
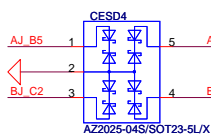
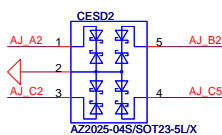


AZALIA JACK

BTX AZALIA CONNECTOR



11NR6-403007-21R



AUDIOB

BLUE

LINE-IN

GREEN

LINE-OUT

PINK

MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

AUDIOA

Orange

CEN/LFE

Black

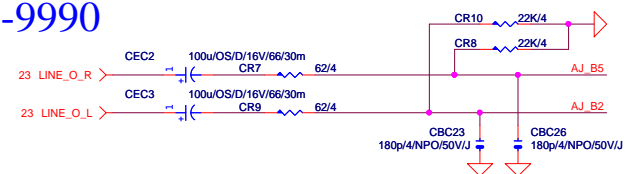
SURROUND

Gray

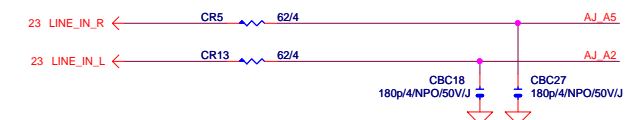
SURROUND SIDE

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

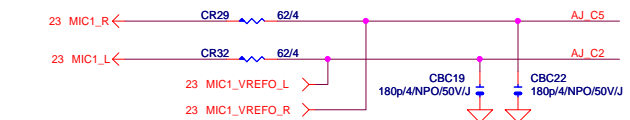
LINE-OUT



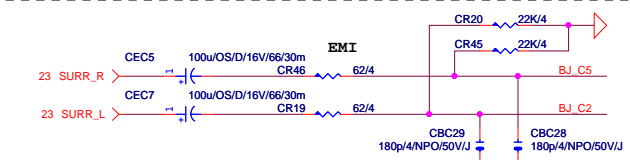
LINE-IN



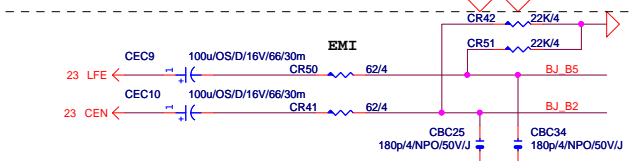
MIC-IN



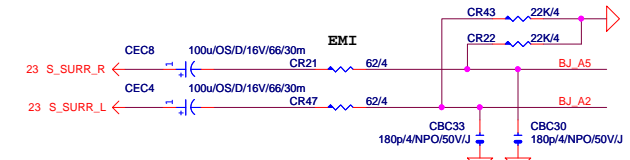
SURROUND



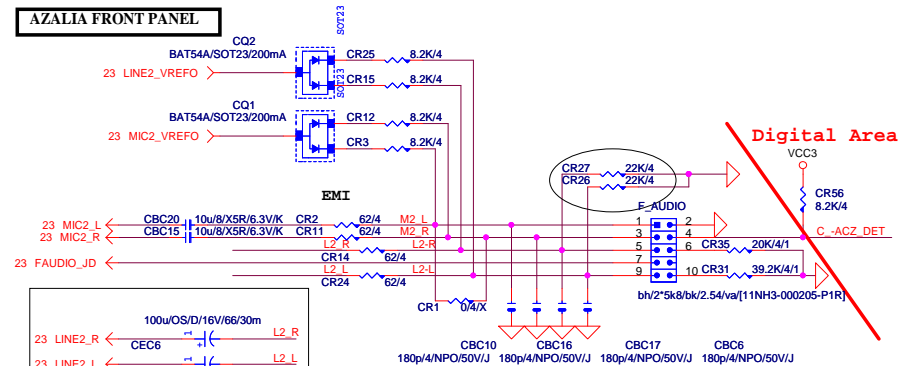
CEN/LFE



SURR BACK



AZALIA FRONT PANEL

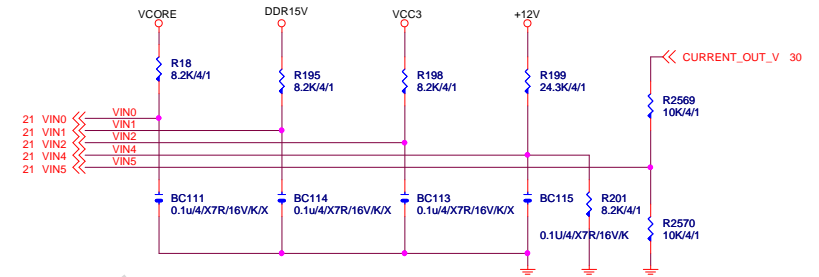
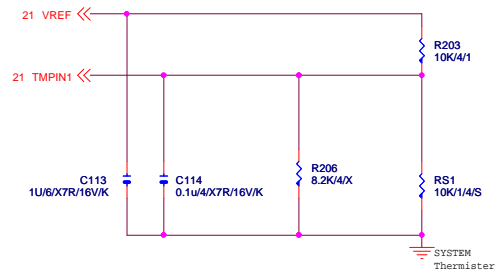


Gigabyte Technology

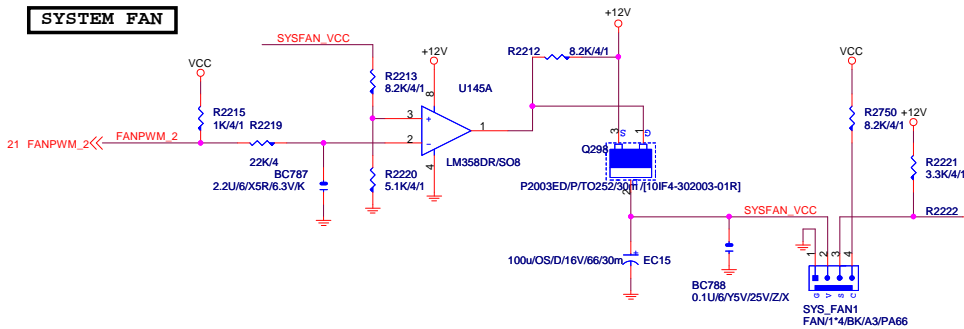
Title		
AUDIO JACK		
GA-990FXA-UD3		
Size	Document Number	Rev
Custom		1.0
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Hardware Monitor circuits

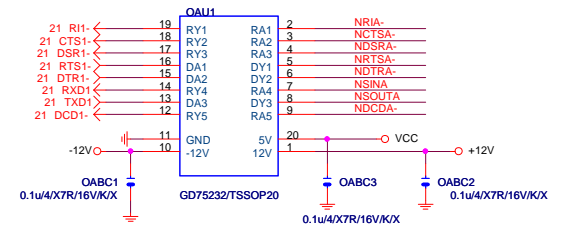
www.xinxunwei.com 400-800-9990



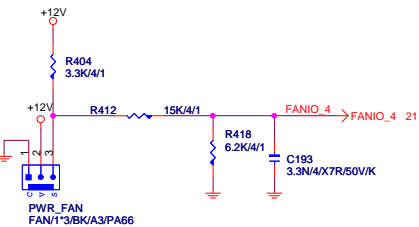
SYSTEM FAN



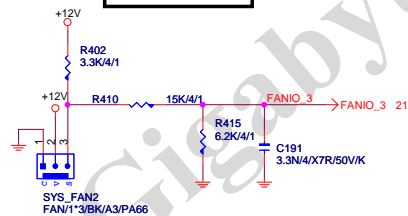
COMA



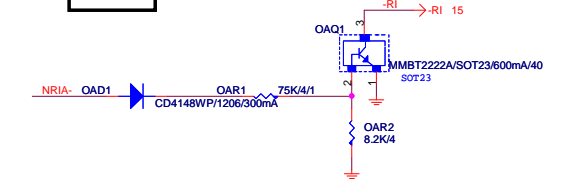
POWER FAN



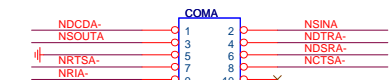
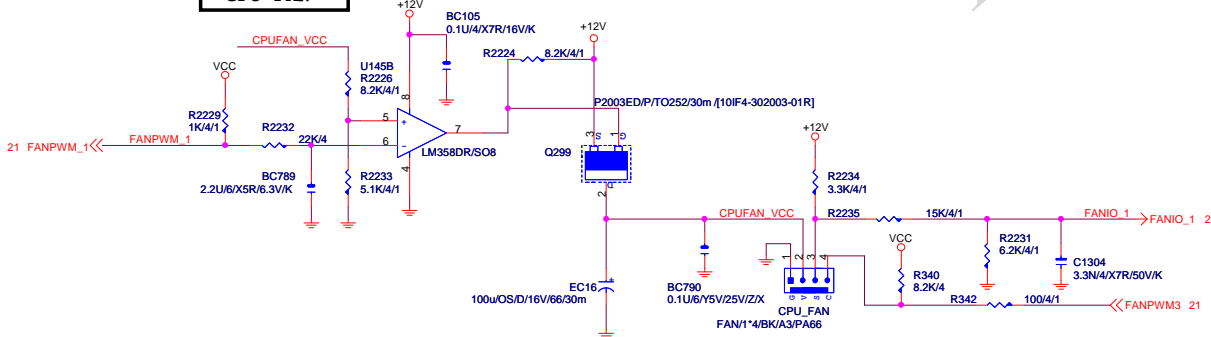
SYSTEM FAN2



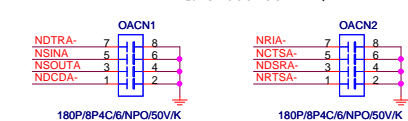
COM RI



CPU FAN

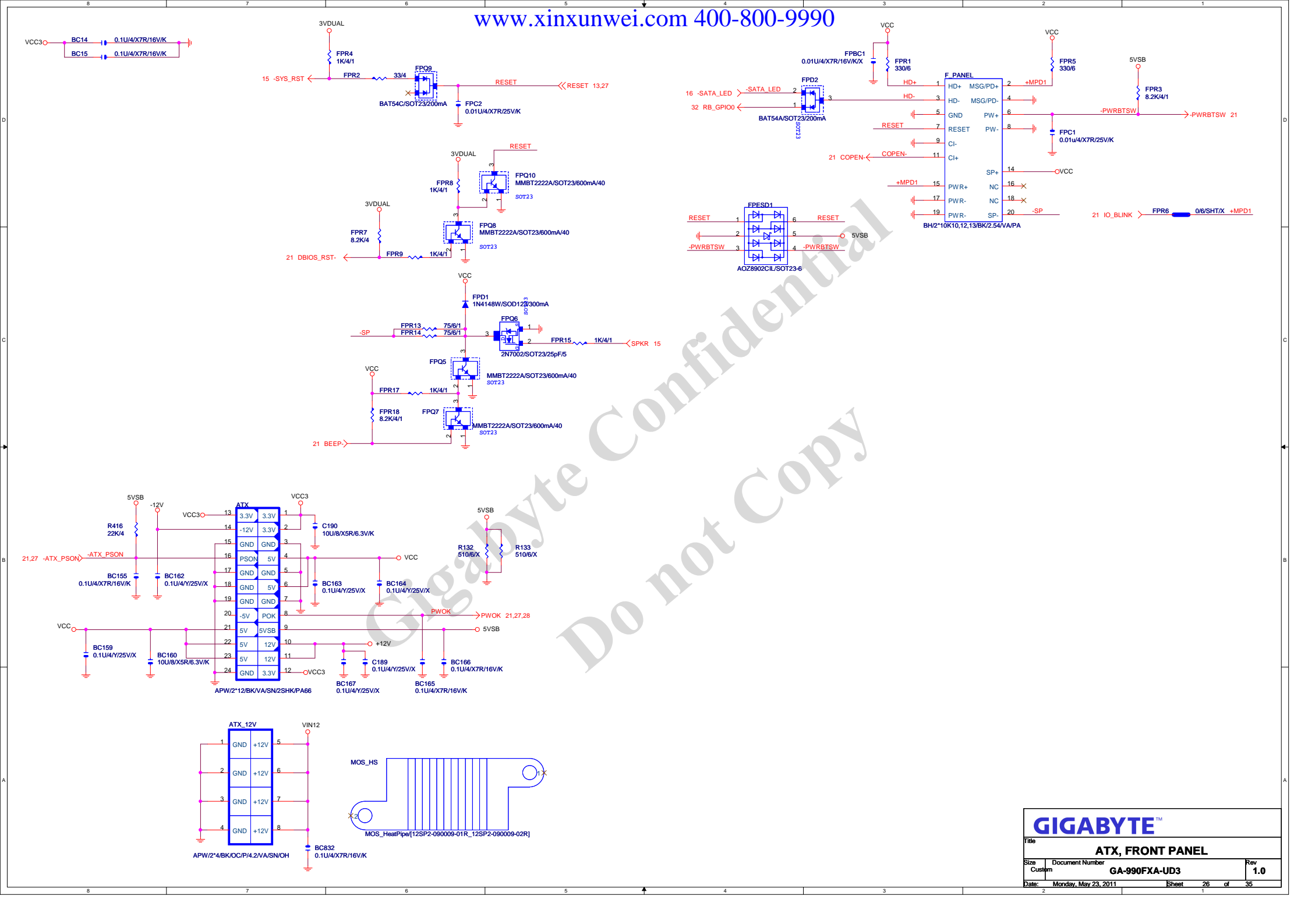


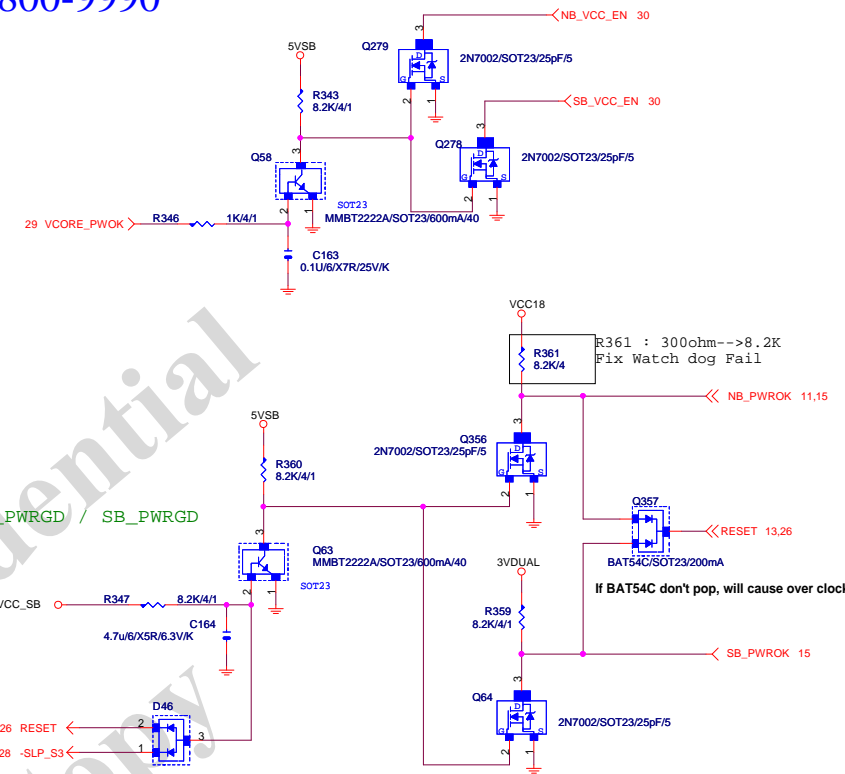
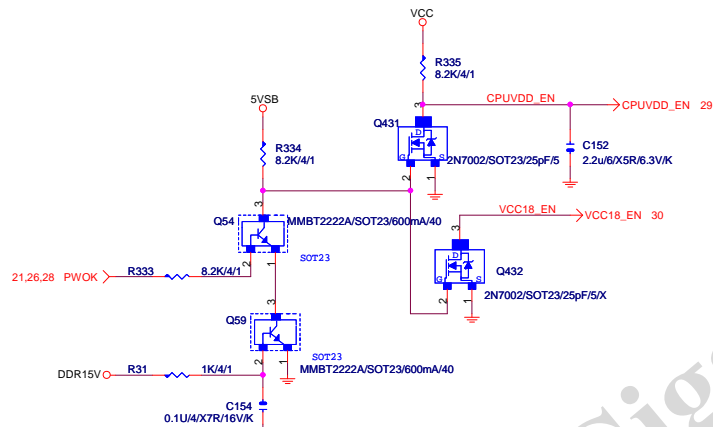
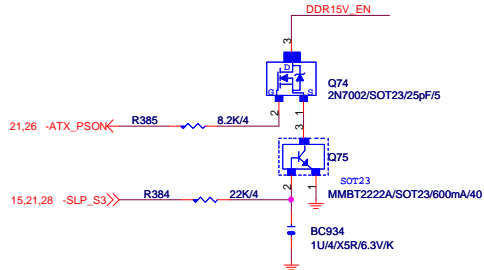
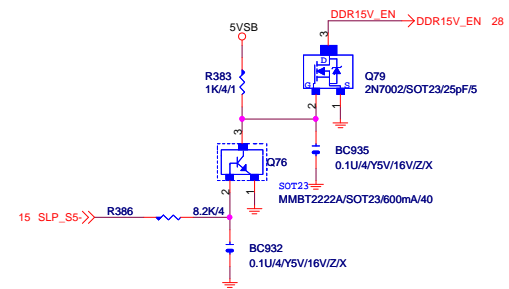
11NH3-000205-Y1R/Y2R



GIGABYTE

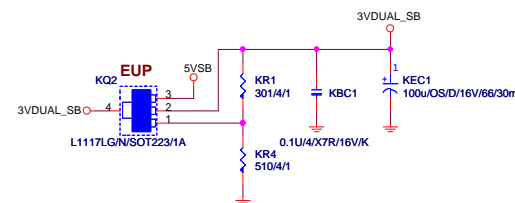
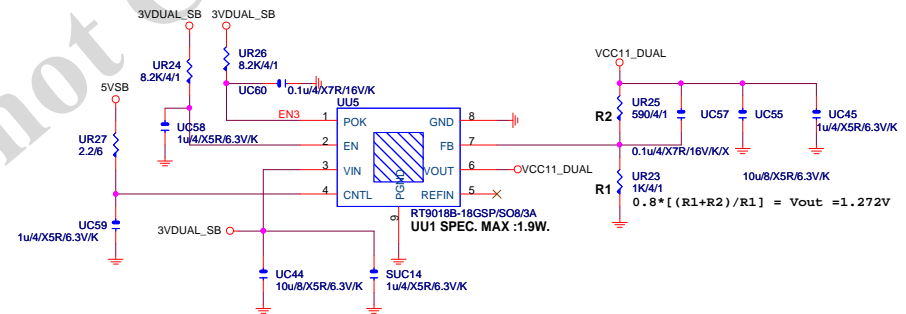
Title		
FAN/HWMO/COM		
Size	Document Number	Rev
Custom	GA-990FXA-UD3	1.0
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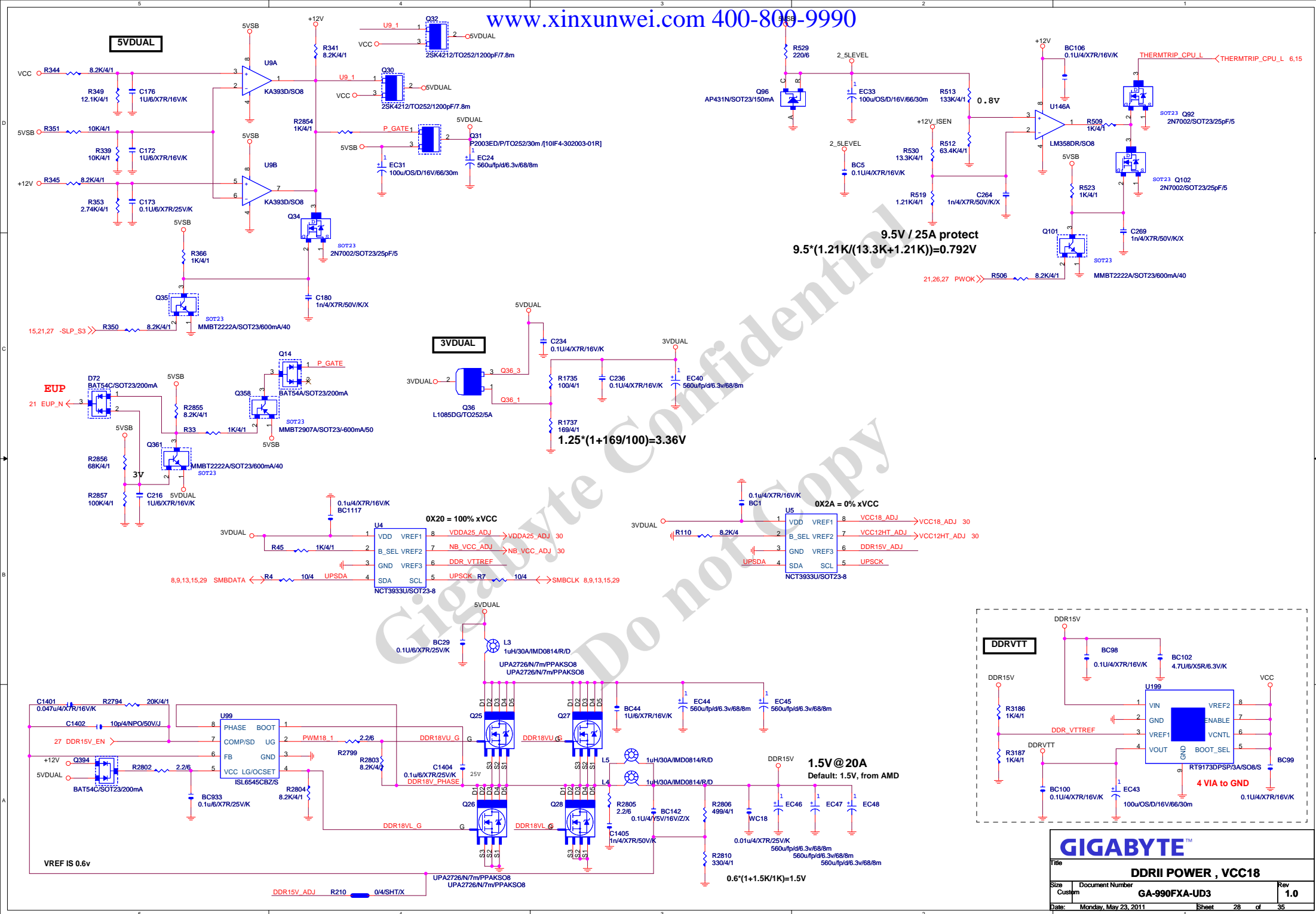
PWOK > NB_PWROK / SB_PWROK

(1.8V , 1.2V , 1.1V) > NB_PWROK 前 1ms

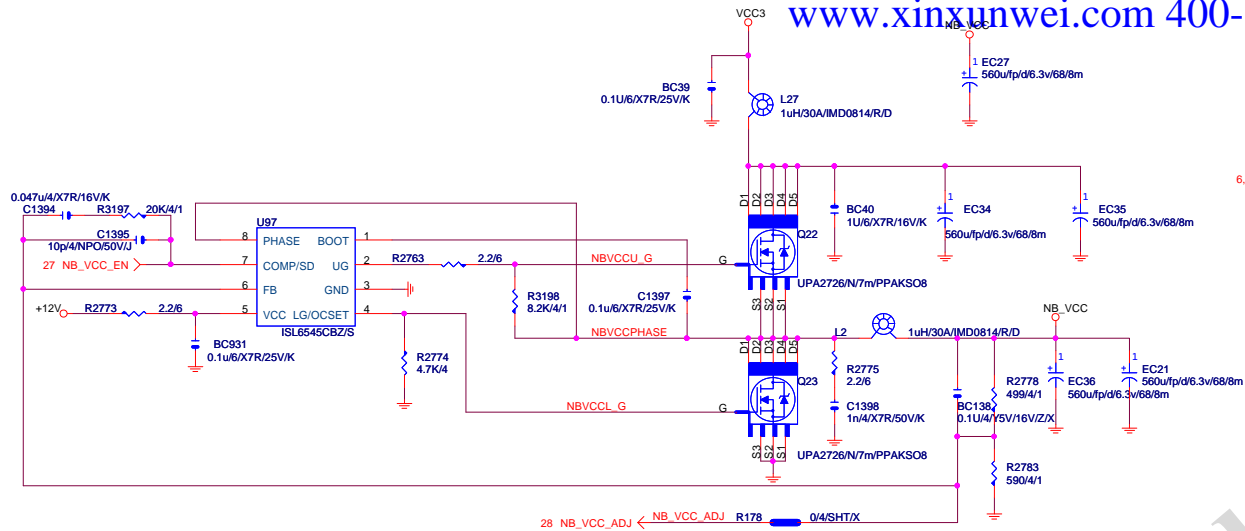


GIGABYTE™

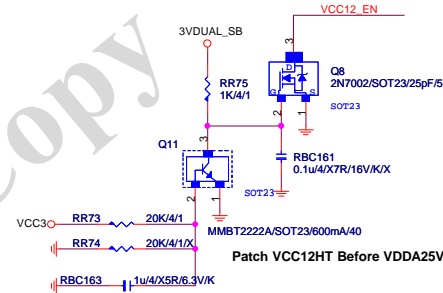
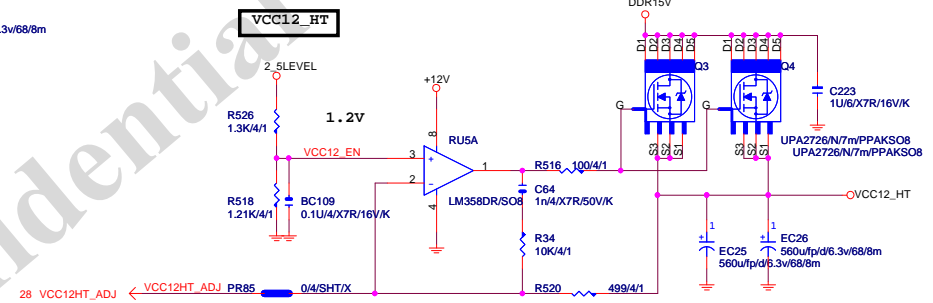
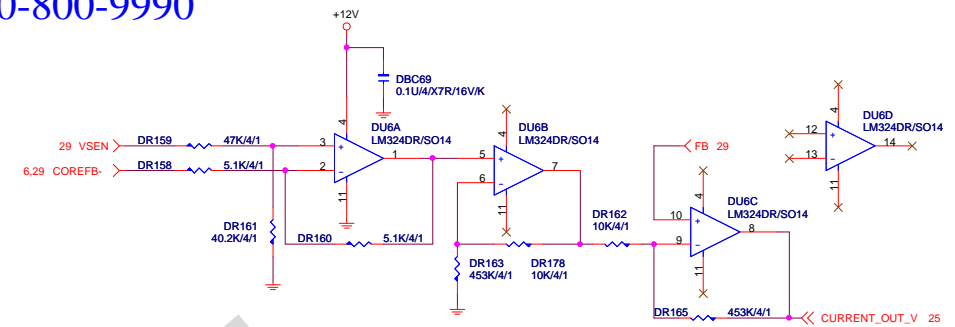
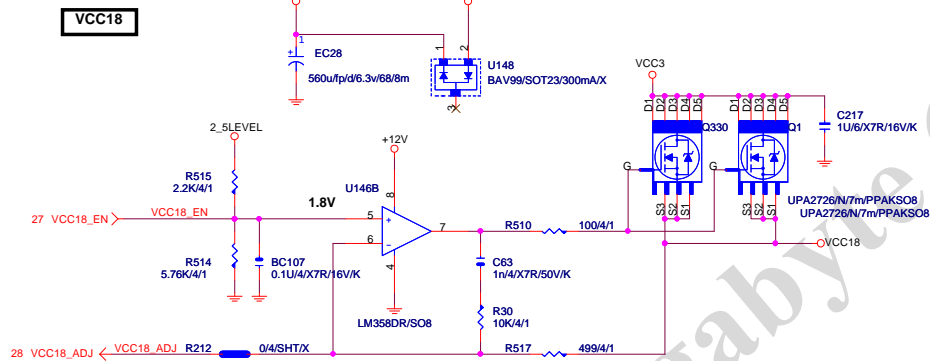
POWER SEQUENCE		
Title	Document Number	Rev
Size	GA-990FXA-UD3	1.0
Custom		
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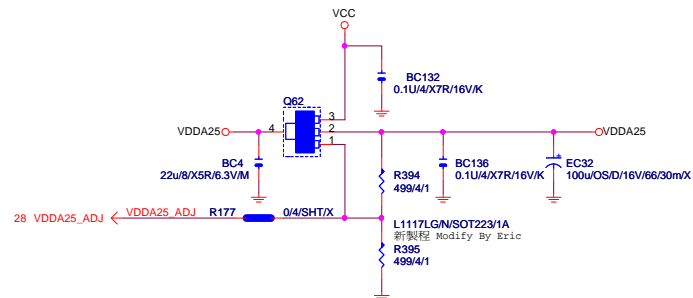
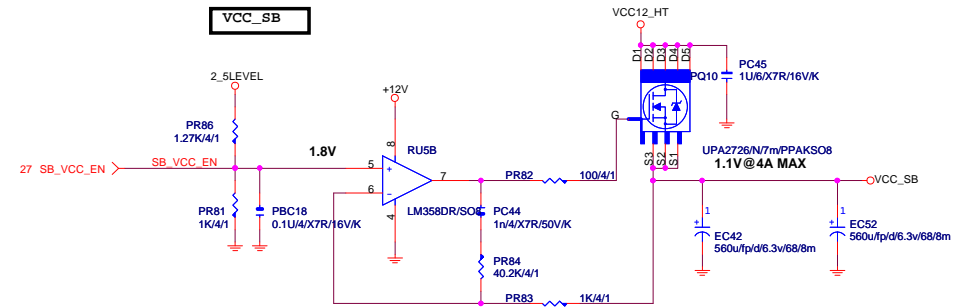


ATI for VCC3/VCC18 power ramp-up 2.1V
U148 for IGP type Only



Patch VCC12HT Before VDDA25V

VCC_SB



GIGABYTE

Title: **NB/SB POWER, VCC12HT, VDDA25**

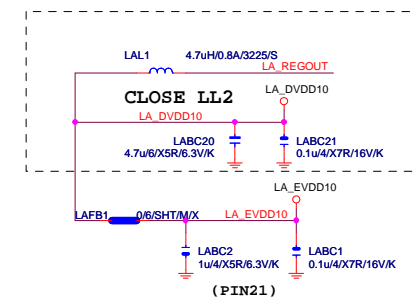
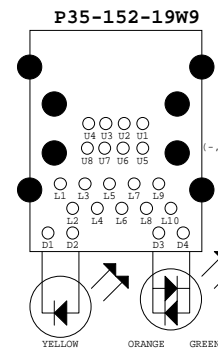
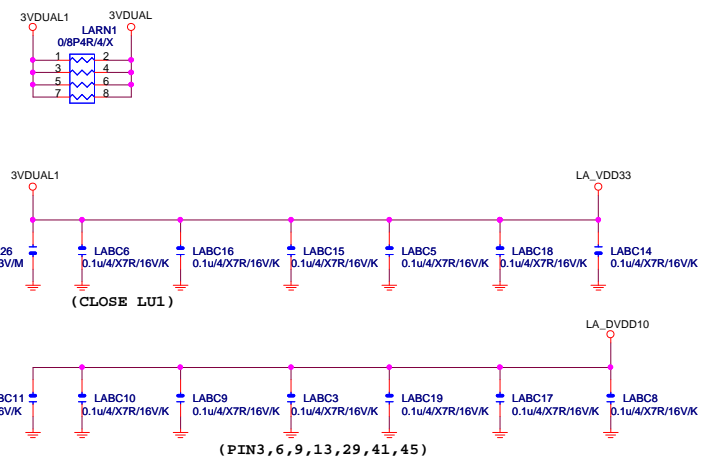
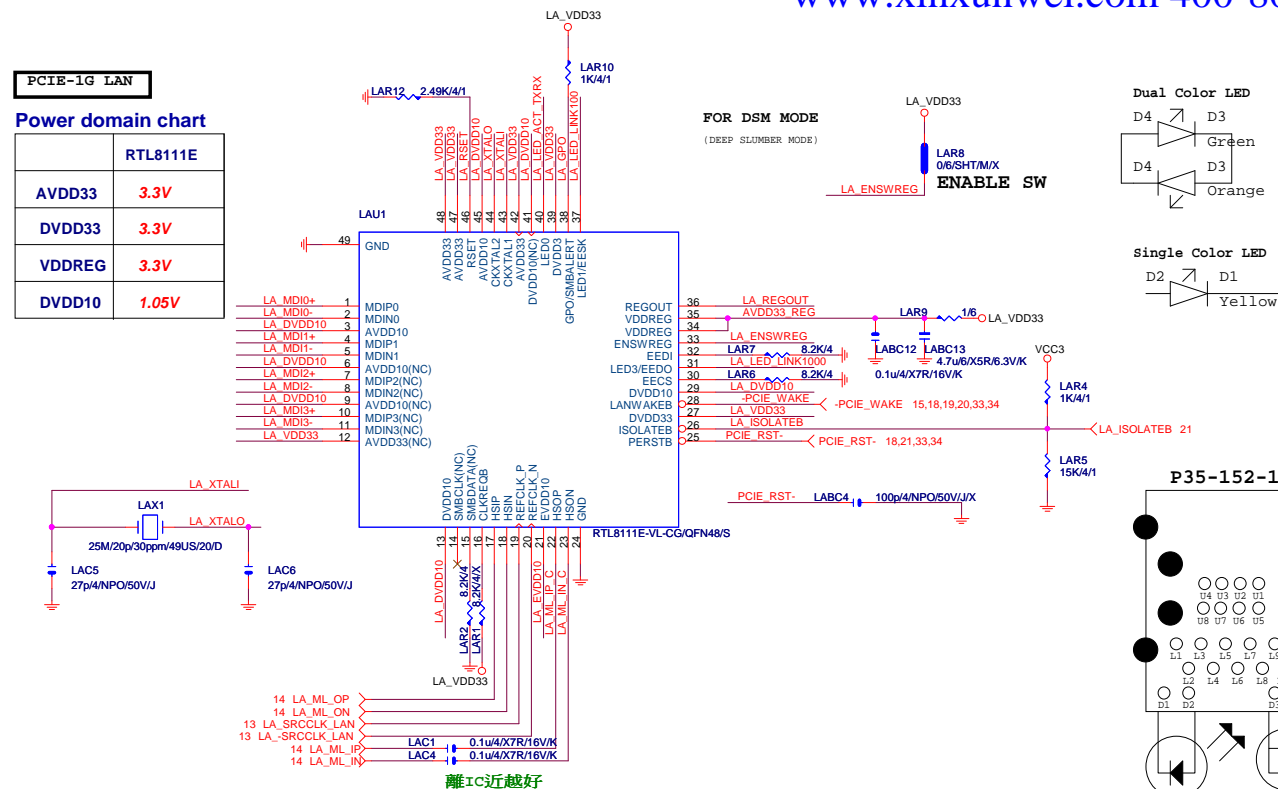
Size: Document Number

Customer: **GA-990FXA-UD3** Rev: **1.0**

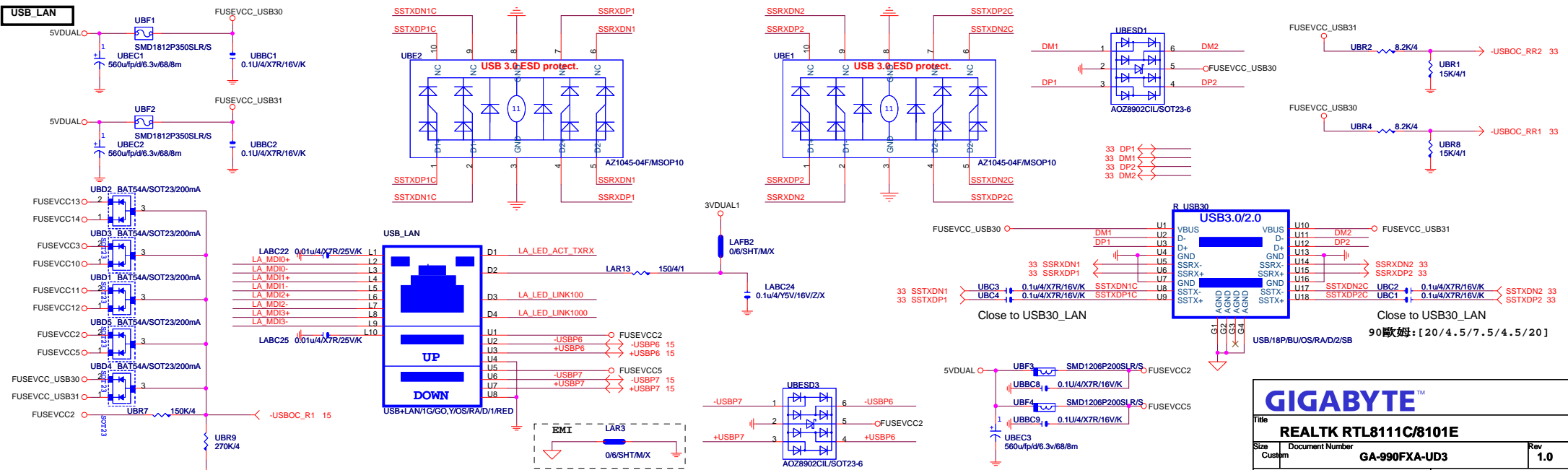
Date: Monday, May 23, 2011 Sheet: 30 of 35

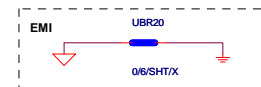
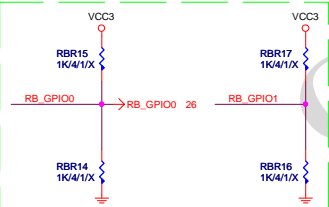
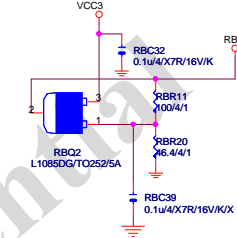
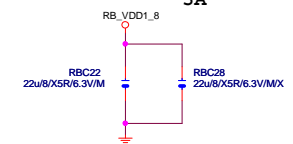
PCIE-1G LAN

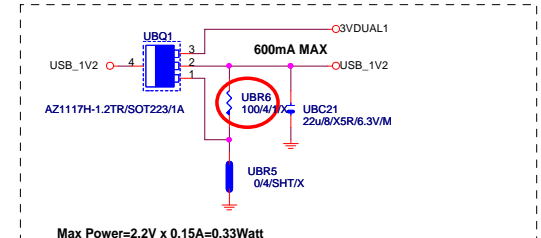
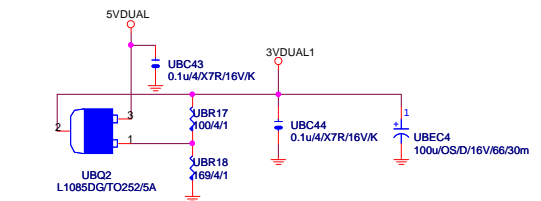
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB_LAN

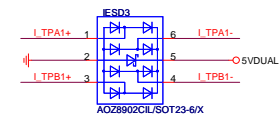
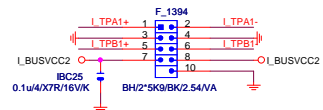
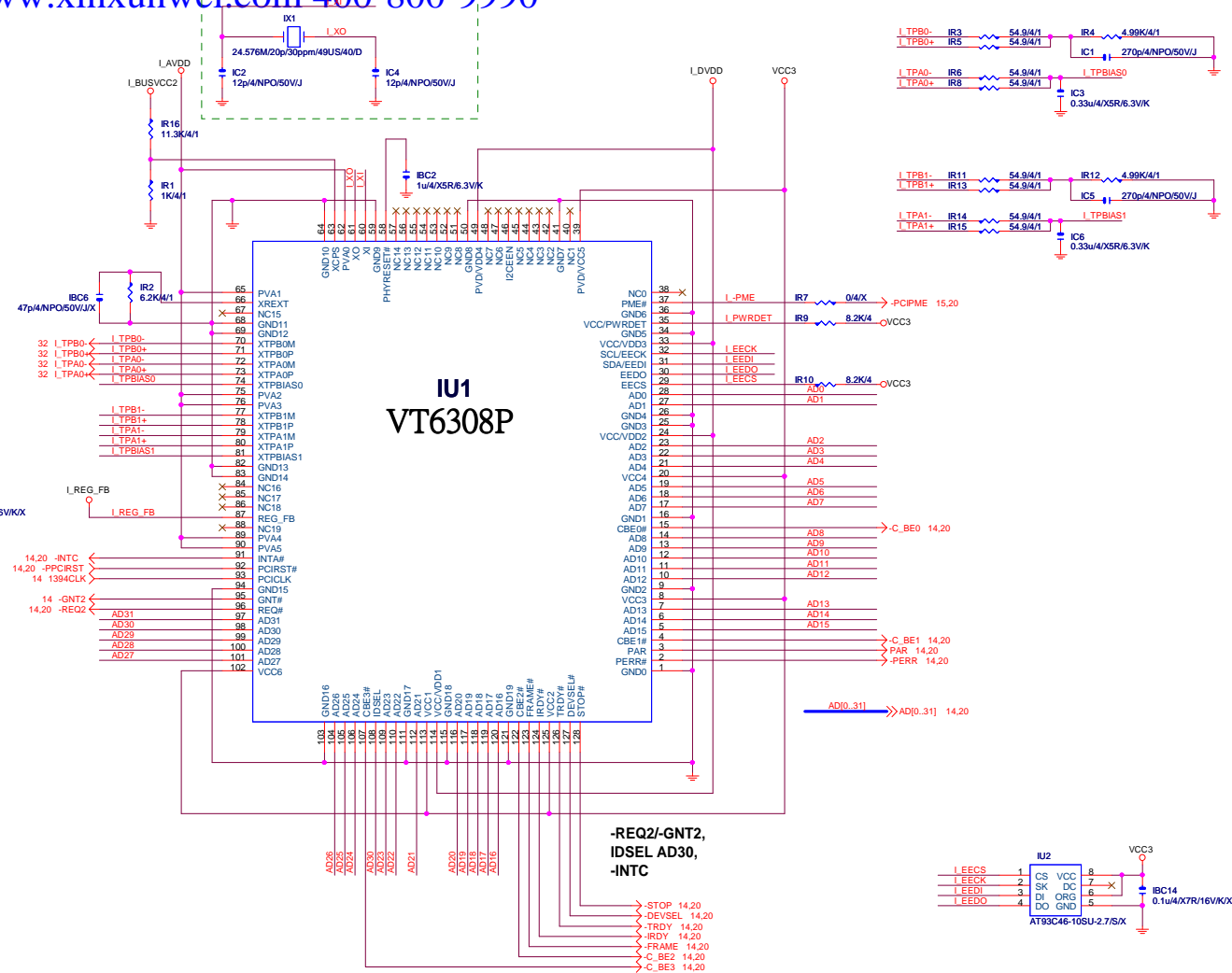
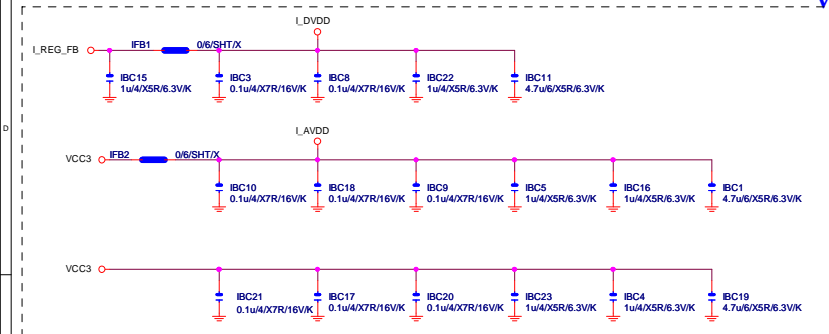




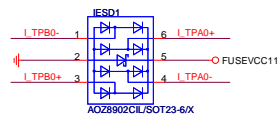


AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]
L1117LG/N/SOT223/1A-->UR17:0/4 ,UR16:100/4/1 [1.25V]

USB3.0 --> 5GHz
BANDWITH=5GHz*(8b/10b)=4Gb/s=500MB/s



Place close to Header or connector



Place close to Header or connector

Gigabyte Technology			
TI TSB43AB23 1394			
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